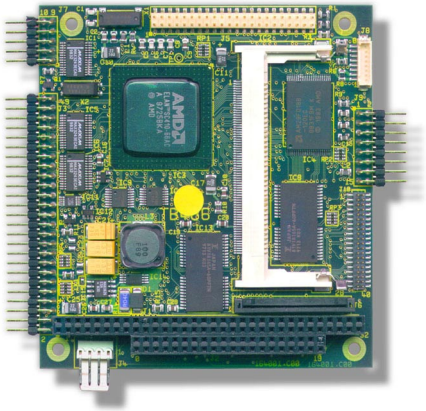
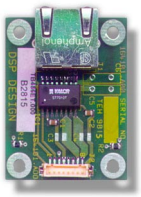
TB486 PC/104 Target Board PC Compatible Computer V2.0 14th October 1998





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1 INTRODUCTION

1.1 OVERVIEW

To maintain our lead in advanced and highly integrated PC compatible computers, DSP Design have released a very highly integrated processor board compliant with the PC/104 V2.3 specification. The board has been specially designed to allow low power operation.

This processor board is fifted with the AMD Elan SC410 high integration processor chip which operates at up to 100MHz. The chip integrates many of the functions commonly found in core logic chips on PC motherboards. It also provides a number of power saving features, including the capability of reducing its clock speed under software control. The board supports up to 64M bytes of DRAM.

It also features the standard PC compatible floppy and IDE disk interfaces, three serial ports, parallel port, keyboard interface, PS/2 mouse port and speaker controllers. In addition, a powerful graphics chip is supplied which can drive both CRT and flat panel displays. A 10Base-T Ethernet interface and analog to digital converter are also provided. The TB486 is a single board PC/104 compatible computer that can operate as a stand-alone module or can be used in a system consisting of a number of other PC/104 modules.

The standard TB486 boards are provided with Flash File System software, which converts the on-board 2M or 4M byte flash chip into a solid-state read/write disk drive.

A range of other PC/104 boards is available from DSP Design. The TC386 and TC486 are lower performance boards, but with the same connectors for interchangeability. The TX486 includes a higher performance 486DX4 processor, but lacks graphics and Ethernet. The TC586 provides a pin-grid-array (PGA) socket for a range of processors, but lacks the floppy and IDE disk interfaces as well as the graphics and Ethernet. The EC586 is a Eurocard design, which incorporates the VGA graphics controller as well as the PGA socket and disk drive interfaces. A wide range of I/O boards is available. Contact DSP Design for up-to-date information on other products in our range.

The TB486 provides connectors with the same pin assignments as other DSP Design processor boards, for easy upgrading.

1.2 TB486 FEATURES

- **High integration processor: a 66MHz AMD Elan SC410 is fifted (a 100MHz chip is available on special order).**
- **PC/104 V2.3 16-bit bus interface for wide compatibility. 0 Floppy and IDE disk controllers.**
- **Three RS-232 serial ports - COM2 is user-configurable as RS-485.**
- **The COM1 serial port can be optionally configured for IRDA-compatible infrared serial communications.**
- **Bi-directional Centronics parallel port. EPP and ECP compatible.**
- **Up to 64M bytes of DRAM. DRAM is implemented with a user-installable 72-pin DIMM module (dual in line memory module). 4M, 8M, 16M, 32M and 64M byte modules are available**
- **2M or 4M byte flash memory for BIOS and solid state disk. (As standard 2M bytes are fifted). A Flash File System is provided with every TB486, to provide a read- write logical disk drive.**
- **Keyboard, PS/2 mouse and sound ports. 0 Chips and Technologies 65550 graphics chip provides VGA graphics on CRT and flat panels at resolutions of up to 1600 x 1280. The chip is connected via the VL local bus for high performance, and 2M bytes of video memory is provided.**
- **Base-T Ethernet chip. The Ethernet magnetics and RJ45 socket are provided on a small PCB (the TB486ET) connected via twisted pair cable to the TB486.**
- **Powered by a single 5V supply. A switched mode power supply is provided to efficiently produce 3.3V for the Elan processor, memory and graphics chips that require this voltage.**

- **A calendar/clock chip uses an external battery.**
- **A 512 byte size serial EEPROM is provided to retain set-up parameters in the absence of an external battery. Space is also available for user data.**
- **Reset, power supply monitor and watchdog timer circuitry.**
- **Expansion is by way of a PC/104 bus which complies with the V2.3 version of the PC/104 bus specification. Some minor restrictions apply to PC/104 bus operation.**
- **The TCDEV Development System provides all the facilities to get your TB486 running quickly, and is recommended for fast product development.**
- **Pin compatible with the TC386, TC486, TX486 and TC586 processors.**

1.3 PC/AT COMPATIBILITY

The TB486 offers an extremely high degree of compatibility with the IBM PC family of computers. This compatibility extends from the MS-DOS level, through BIOS-level compatibility to register-level compatibility.

• The processor used on the TB486 board includes on-chip peripherals - timers, interrupt controller, DMA controller etc. These are software compatible with equivalent Intel peripheral chips used on the original IBM PC and PC/AT. The Elan chip provides other features. A calendar/clock circuit and speaker port are included, and the chip looks after clock generation, address decoding, expansion bus timing, memory mapping and various other functions.

Around the Elan chip DSP Design has integrated floppy and IDE disk controllers, a keyboard and mouse controller, three serial ports and a Centronics parallel printer port. These peripherals are software and hardware compatible with the IBM PC/AT.

The 65550 graphics chip provides VGA, SVGA and XVGA compatible graphics. Windows drivers provide access to the high performance BITBLT graphics engine within the chip. The Ethernet chip is also provided with drivers for a range of operating systems.

1.4 PC/104 AS A PC EXPANSION BUS

Users can operate the TB486 as a single board computer. If expansion is required I/O boards can be accessed via the PC/104 interface provided on the TB486.

The PC/104 bus is a compact version of the IEEE P996 (PC and PC/AT) bus, optimized for embedded systems applications. DSP Design and other PC/104 manufacturers offer a wide range of I/O boards that will work with the TB486, in the same manner that a conventional PC can be enhanced by the addition of expansion boards.

The PC/104 I/O board range includes analogue and digital I/O cards, serial comms, local area network boards and other specialist functions. DSP Design manufactures a number of PC/104 modules and is committed to expanding this range.

It is the policy of DSP Design to introduce, where appropriate, new PC/104 I/O cards which are software compatible with similar cards for the PC. This has the tremendous advantage of allowing users to make use of the software that has already been written for PC expansion cards.

1.5 THE TB486 ARCHITECTURE

The block diagram in Figure 1 shows the architecture of the TB486. The Elan processor accesses DRAM and the graphics chip on a fast local bus. It also provides a slower PC/104 bus (ISA bus), on which the Flash memory, Ethernet and Super I/O chips are located. The Elan chip performs a range of house-keeping and glue logic functions, as well as providing timer, interrupt, DMA, speaker and memory mapping facilities. The Super I/O chip includes the floppy and IDE disk controllers, serial and parallel I/O functions as well as the keyboard and mouse controller.

Finally a 16-bit PC/104 interface allows the TB486 to perform memory and I/O accesses to the PC/104 bus. The Elan interrupt and DMA controllers are used by the on-board peripherals as well as being connected to the expansion bus.

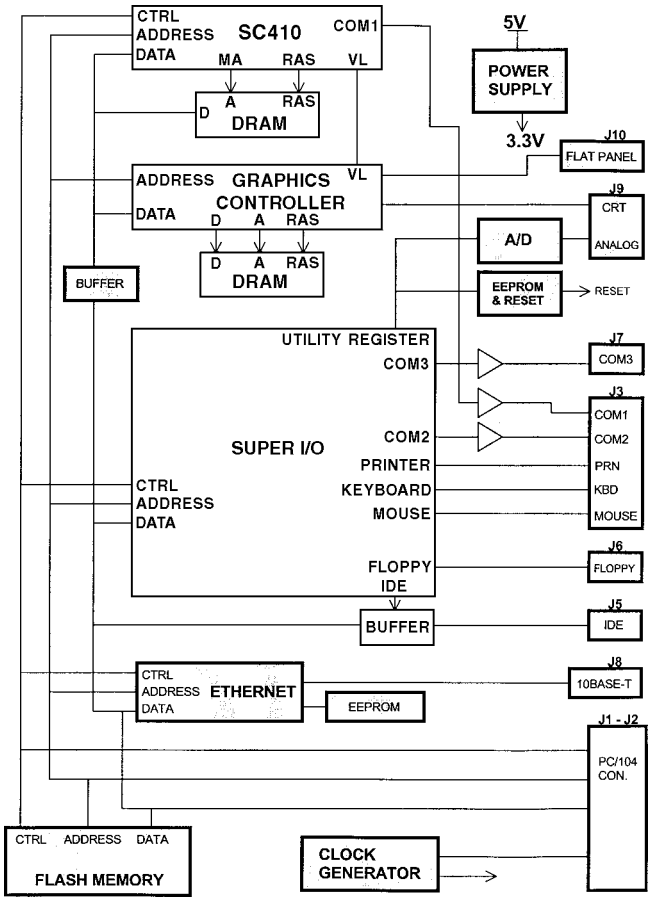

FIGURE 1 - TB486 BLOCK DIAGRAM

1.6 GETTING STARTED QUICKLY

This manual gives all of the information that most users will need in order to operate the TB486. This section gives a quick introduction to getting started. More details on configuring the board are given in Appendix B: TB486 Setup Procedure. Those people who have special requirements may require further information. If this is the case our support engineers will be pleased to help you, but please read the manual first.

DSP Design strongly recommend developing with the TCDEV Development System, as in our experience this significantly reduces development time and users' technical problems.

•The TCDEV is a PC/104 based development platform. It has sites for two PC/104 expansion cards. These sites are arranged so that both sides of the PC/104 boards can be accessed by engineers. The TCDEV's features include an on board VGA graphics controller with 15 pin VGA connector, a floppy and hard disk controller, a floppy drive plus cable, a small prototyping area, a full PC/AT slot for interfacing standard PC and PC/AT bus cards to the PC/104 bus and a battery for CMOS RAM backup. The TCDEV has all the standard PC connectors for interfacing to the outside world. These include two serial port 9 way D-type connectors, a parallel port 25 way D-type connector, a 5 pin DIN keyboard connector and a PS/2 style mouse connector.

DSP Design also supply the TCPSU which is a compact 3OW power supply with cabling to make it easy to use with the TCDEV.

Most users will find getting started with the TB486 and TCDEV simplicity itself. The TB486 plugs directly onto the TCDEV and a 50-way ribbon cable connects the TB486 J3 I/O socket to the TCDEV I/O socket. This links the COM1 and COM2 serial ports, parallel port, keyboard, mouse etc onto the TCDEV and in turn to the PC compatible connectors mounted on the edge of the TCDEV board.

The TB486 includes its own VGA, floppy and IDE disk controllers. VGA, floppy and [DE disk controllers are also present on the TCDEV. It is possible to use disk controllers on the TB486 or the controllers on the TCDEV (though not a mixture of both). Similarly, it is possible to use the VGA controller on the TCDEV or on the TB486. These instructions assume that the VGA and disk controllers on the TCDEV are used, since this will simplify connections.

The TCDEV has its own Technical Reference Manual.

There are two styles of TCDEV in the field. The REV B TCDEV boards can be identified by having only one site for PC/104 boards, and only one power LED. The REV D and later TCDEV boards have two sites for PC/104 boards, and eight LEDs in a row as well as the power LED. The next two sections describe operation with each of the TCDEV variants.

1.6.1 USING REV B TCDEV DEVELOPMENT SYSTEM

To use the system, first install a DRAM DIMM module into the TB486 DRAM socket, observing its polarity, and observing proper anti-static precautions. The DIMM socket has a lug which engages with a cut-out on the module, which prevents incorrect installation.

Enable the disk controllers and VGA graphics on the TCDEV. This is done by setting the three jumpers at jumper areas E3, E4 and E5 to the “EN” position. Ensure there are jumpers between positions 1 & 12, and 4 & 9 at jumper area El. The battery back- up jumper should be set between positions 1 & 2 at E2. Ensure that the TCDEV IC5 socket contains a VGA BIOS EPROM.

Plug the TB486 onto the TCDEV and connect the J3 I/O connector between the two boards. Ensure that pin 1 of the TCDEV 50-way connector J3 goes to pin 1 of the TB486. Failure to connect the 50-way cable correctly may damage the equipment.

Connect but do not switch on the TCPSU. (Note that the TCPSU power connector is polarized. Ensure that the locking tab on the power supply cable mates with the locking tab on the TCDEV connector).

Connect the power supply earth wire to an earth spade terminal. Failure to connect the power supply cable assembly correctly may damage the equipment.

Connect the keyboard and VGA monitor to TCDEV connectors J7 and J13 respectively.

Insert a floppy disk containing DOS into the TCDEV floppy disk drive and switch the power supply on. The computer should boot DOS from the floppy disk.

• Reset the computer, and this time hit the F2 key on the keyboard to enter the BIOS Setup menu. You should familiarise yourself with the Setup options (see section 6.2 for guidance). End by saving the setting to CMOS memory.

You will soon want to experiment with the TB486 on-board peripherals - floppy and IDE disk controllers and VGA controller. The floppy and IDE disk controllers must be disabled with the E5 and E4 jumpers on the TCDEV, and the TB486 on-board floppy and IDE disk controllers must be enabled by entering the Advanced/integrated Peripherals menu in the Setup program. The TCDEV VGA controller is disabled at the E3 jumper.

When fitting an IDE disk drive, whether on the TCDEV or the TB486, you will need to set the drive parameters using the Setup program. This is done using the Main/IDE Adapter 0 Master menu. Section 3.7 has more details on the IDE interface.

•A Flash File System is also provided with the TB486, giving you a solid-state disk drive of just under 2M byte capacity.

(The default is for 2M bytes of Flash memory; the TB486 can be fitted with 4M bytes as a special order). When you receive your TB486 the Flash File System drive will be formatted, but does not yet contain an operating system. Section 6.6 has details of the Flash File System.

•When development is complete the TB486 is removed from the TCDEV Development System. It can then operate stand-alone, or be used with other PC/104 modules. As part of your development process you may well need to change the BIOS, and alter Setup settings and save them in the serial EEPROM. These steps are described in this manual.

1.6.2 USING REV D OR LATER TCDEV DEVELOPMENT SYSTEM

To use the system, first install a DRAM DIMM module into the TB486 DRAM socket, observing its polarity, and observing proper anti-static precautions. The DIMM socket has a lug which engages with a cut-out on the module, which prevents incorrect installation.

Enable the disk controllers and VGA graphics on the TCDEV. This is done by setting the three jumpers at jumper areas E3, E4 and E5 to the “EN” position. Ensure there are jumpers between positions 1 & 12, and 4 & 9 at jumper area El. The battery back- up jumper should be set between positions 1 & 2 at E2. The status LED jumpers at E7 should both be set in the 1 - 2 position. At jumper area E6 set all jumpers to the DIS position, except the jumper labeled C000, which should be set to the EN position.

Plug the TB486 onto the TCDEV and connect the J3 I/O connector between the two boards. It is probably best to use the J15 and J16 PC/104 connectors, and mount the TB486 face up, but you can also use the Jl and J2 connectors, and mount the TB486 face down. In either case ensure that pin 1 of the TCDEV 50-way connector J3 goes to pin 1 of the TB486. ***Failure to connect the 50-way cable correctly may damage the equipment.***

Connect but do not switch on the TCPSU. (Note that the TCPSU power connector is polarized. Ensure that the locking tab on the power supply cable mates with the locking tab on the TCDEV connector).

Connect the power supply earth wire to an earth spade terminal. On REV D TCDEVs this terminal is soldered to the printer connector. Failure to connect the power supply cable assembly correctly may damage the equipment.

Connect the keyboard and VGA monitor to TCDEV connectors J7 and J13 respectively.

Insert a floppy disk containing DOS into the TCOEV floppy disk drive and switch the power supply on. The computer should boot DOS from the floppy disk.

Reset the computer, and this time hit the F2 key on the keyboard to enter the BIOS Setup menu. You should familiarise yourself with the Setup options (see section 6.2 for guidance). End by saving the setting to CMOS memory.

You will soon want to experiment with the TB486 on-board peripherals - floppy and IDE disk controllers and VGA controller. The floppy and IDE disk controllers must be disabled with the E5 and E4 jumpers on the TCDEV, and the TB486 on-board floppy and IDE disk controllers must be enabled by entering the Advanced/Integrated Peripherals menu in the Setup program. The TCDEV VGA controller is disabled at the E3 jumper. In addition, the C000 jumper at the E6 jumper area must be disabled.

When fifting an IDE disk drive, whether on the TCDEV or the TB486, you will need to set the drive parameters using the Setup program. This is done using the Main/IDE Adapter 0 Master menu. Section 3.7 has more details on the IDE interface.

A Flash File System is also provided with the TB486, giving you a solid-state disk drive of just under 2M byte capacity. (The default is for 2M bytes of Flash memory; the TB486 can be fitted with 4M bytes as a special order). When you receive your TB486 the Flash File System drive will be formatted, but does not yet contain an operating system. Section 6.6 has details of the Flash File System.

When development is complete the TB486 is removed from the TCDEV Development System. It can then operate stand-alone, or be used with other PC/104 modules. As part of your development process you may well need to change the BIOS, and alter Setup seftings and save them in the serial EEPROM. These steps are described in this manual.

2 PROCESSOR AND MEMORY

The TB486 single board computer is based around the AMD Elan SC410 processor chip. There is one DIMM DRAM socket. The standard TB486 is supplied without memory, allowing you to choose memory to suit your application. DRAM options are detailed in Appendix D, Options and Ordering Information.

2.1 PROCESSOR

The TB486 is based on the AMD Elan SC410 processor chip. This is a highly integrated chip which includes an x86 compatible processor and many integrated peripherals. It includes all of the motherboard support circuits used in PCs.

The processor is similar to the 80486, with an 8k write-back Ll cache. The Elan does not contain a floating point processor. It runs at up to 100MHz (although a 66MHz chip is fifted as standard), but the processor clock speed can be set to trade off computing power against power consumption.

The integrated peripherals include two 8237 compatible DMA control units (7 channels), one 8254 compatible timer control unit (3 channels), two 8259 compatible interrupt control units (15 interrupts), AT port logic and an MC146818 compatible calendar/clock and CMOS RAM chip (although the real-time clock in the Super I/O chip is used instead). The majority of the peripheral functions are the same as on all IBM PC/AT compatible computers. This includes the timers, interrupt controllers and DMA controllers as well as registers such as the NMI and speaker inhibit registers, fast reset and A20 gate registers. Software which accesses the IBM PC/AT peripherals will have the same effect when running on the TB486, giving rise to a high degree of PC-compatibility.

The other housekeeping functions provided by the Elan are:

- Memory controller with on-board memory mapping registers
- DRAM memory controller
- Clock generation logic 0 VL bus for graphics controller
- PC/104 bus interface and conversion logic
- Peripheral I/O address decoding
- Power management logic.

The Elan includes a number of in-built peripheral circuits, some of which are used in the TB486 and some of which are not. Aside from the timers, interrupt controllers and so forth, the only peripheral which is used is the serial port (COM1) with an optional IRDA mode.

- The peripherals which are not used are:
- Real-Time Clock
- LCD graphics controller
- Keypad interface
- XT keyboard controller
- PCMCIA controller
- Printer port

The Elan chip also includes a number of internal configuration registers. These registers are unique to the Elan chip. They control timing on the expansion bus, shadow RAM, DRAM configuration, memory mapping, power management and so forth. They are initialized by the BIOS and will not normally need to be accessed by the user.

The performance of the TB486 may be gauged by the processor performance ratings produced by the Norton Si and the Ziff-Davis WinBench 98 programs as shown in Table 1. For comparison purposes the table also contains the measurements for a 100MHz 486DX4 (as used in DSP Design's TX486 board). This shows that at a comparable CPU speed the Elan processor is faster than the 486DX4.

CPU Frequency	Norton SI Rating	Winbench 98 Rating 32-bit
8MHz	12.8	Test not performed
16MHz	25.6	Test not performed
33MHz	51.1	45.5
66MHz	103.8	60.2
100MHz	155.8	66.7
486DX4-100	156.5	59.8

TABLE 1 - TB486 PERFORMANCE RATINGS

The above measurements were made with an 8-chip 16M byte DIMM module installed. The Si program was run using MS-DOS and the WinBench Program was run using Windows 95. Power management was switched off.

Users should make their own decision concerning cooling of the processor. The processors will dissipate about 1.8W at 100MHz, 1.2W at 66MHz and about 700mW at 33MHz, and may get quite hot. AMD recommends a heat sink and/or a fan, at least when the processor runs at 100MHz and 66MHz, to keep the temperature of the processor down. In addition, the cooler a chip is the more reliable it will be. A fan or fan and heatsink combination can be fitted to the processor, or a fan could be provided in the enclosure along with the PC/104 boards. DSP Design can provide heatsinks. See Appendix D for ordering information.

As an alternative the enclosure could be designed so that part of the enclosure acted as the heat sink. Thermal materials are available to provide a good thermal bond between the CPU and the case.

Another alternative is to use Chomerics T-Wing flexible heat spreader product. The TB486 includes a built-in temperature sensor, which can be used to measure the temperature. This may be useful in formulating a temperature management strategy.

2.2 CLOCK

The Elan includes a 32.786kHz oscillator circuit that is used for the real-time clock. This oscillator is used as the reference frequency for four phase-locked loop (PLL) clock synthesiser circuits which generate internal frequencies used by different sections of the Elan chip.

The clock synthesisers are:

- Intermediate PLL - used to provide an input to the following the PLLS.
- Low-speed PLL - used for UART and timer.
- Graphics PLL - internal LCD graphics controller, not used in the TB486.
- High-speed PLL - used for CPU, DRAM, ISA bus controller.

The CPU itself runs as standard at 33MHz, but this frequency can be changed by software. The clock speed can be increased to 66MHz or 100MHz (so-called “Hyper- Speed” mode) to improve processing speed, using yet another PLL clock synthesiser. (The standard TB486 is fifted with a 66MHz processor. In practise this chip’s speed can be increased to 100MHZ, but the due to the rating of the Elan processor fifted, and the need for a different power supply voltage at 100MHz, reliable operation of the TB486 at this speed cannot be guaranteed. If you require 100MHz operation then 100MHz boards can be produced by special order). The clock speed can also be reduced, and even stopped, to save power. Frequencies of 16MHz, 8MHz, 4MHz, 2MHz and 1 MHz are possible. These can be set by using the Setup menu.

If automatic power saving is enabled then the clock speed will be adjusted automatically by software in order to reduce power consumption. Section 7 describes the clock changes. A clock generation circuit exists outside the processor chip.

This produces the following clocks:

- A 14.318MHz clock which is routed to the PC/104 bus as the OSC signal, and to the 65550 graphics chip where it is used to derive all graphics and DRAM timing. The 14.318MHz clock is divided by 12 to produce a 1.19MHz clock. This is sent to the Elan chip where it is used as an input to the counter/timers.
- An 8MHz clock which is routed to the PC/104 bus as the BUSCLK signal. Note that this clock is free-running and is not synchronised to the PC/104 bus cycles performed by the processor.
- A 24MHz clock which is sent to the Super I/O chip, for the floppy disk controller and serial ports.
- A 20MHz clock which is used by the Ethernet controller chip.

This clock generation circuit can be switched off, as a power saving measure, if so desired, although those sections of circuitry which use this clock generator will of course loose their clocks and consequently will not be able to operate. See section 7 for details of power saving options.

2.3 DRAM

The main memory of the TB486 consists of Dyrramic RAM (DRAM) chips. The chips are mounted on a small 72-pin printed circuit board called a DIMM module (dual-in-line memory module). The memory is 32-bit wide.

Five options are available:

- 4M bytes
- 8M bytes
- 16M bytes
- 32M bytes
- 64M bytes

The standard configuration of the TB486 is to have no DRAM fitted. DIMM modules must be ordered separately and fitted into the DIMM socket on the TB486. See Appendix D: TB486 Options and Ordering Information.

The use of DIMM modules for DRAM memory means that the DRAM configuration can be altered at a later stage. DSP Design carry stock of the DIMM modules described above, or customers may provide their own. Note that the DIMM modules are 3.3V. The 5V DIMM modules used on other DSP Design processors are not suitable. EDO or FPM modules may be used. EDO modules will give better performance. DRAM of 70ns or faster should be used.

Care must be taken when handling the TB486 and the DIMM memory modules. Ensure that all anti-static handling precautions are taken. See Appendix B: TB486 Setup Procedure for instructions on installing DIMM modules.

Note that only the first 640k bytes of DRAM are usually directly accessible by DOS. Some of the remaining DRAM is used to shadow the BIOS (see section 6.1) and the remainder is re-mapped above the 1M byte boundary, where it can be used by DOS extenders and by Windows and other operating systems.

The BIOS automatically determines the amount of DRAM present and configures the internal Elan registers accordingly.

Memory between C0000H and FFFFFH (the top of the 1 M byte block) can be used to shadow BIOS code. This allows the BIOSes to run at the fast DRAM speed rather than the slow EPROM speed. Typically the system BIOS (from F0000H - FFFFFH), the VGA BIOS (from C0000H - C9FFFH) and the Flash File System (from CC00OH - CFFFFH) driver are shadowed. Memory beyond the 1M byte limit is available for Windows and other protected mode operating systems.

2.4 FLASH MEMORY

The TB486 is fifted with one 2M byte AMD or Fujitsu 29F016 Flash memory chip. (The default is for 2M bytes of Flash memory; the TB486 can be fifted with 4M bytes as a special order).

Flash memory is non-volatile memory which can be programmed while it is soldered to the TB486. Data written to the Flash memory is retained after power is removed.

The Flash memory serves two purposes. Firstly, it contains the BIOS: machine-dependent software that is required to run an operating system.

•The second function of the Flash memory is to provide a Flash File Systems for users who want a solid state disk.

The top 128k bytes of the Flash chip are used for the system BIOS and any BIOS extensions, such as the VGA BIOS extension and the Flash File System BIOS extension. The TB486 comes pre-programmed with a system BIOS, a VGA BIOS extension for on-board 65550 graphics controller and a Flash File System BIOS extension. See section 2.5 for more information on memory mapping of the TB486, and section 6.3 for more information on BIOS extensions.

A Flash File System is provided with every TB486. This converts the remaining 1920k bytes of the 2M byte Flash chip into a non-volatile read-write logical disk drive. This Flash disk can contain the MS-DOS operating system as well as your application program. The Flash File System is described in section 6.6.

Utility programs are provided on the TB486 Utility Disk which allow the Flash chip to be programmed by the user. This allows the user to program various alternative BIOS image files into the Flash memory. These utility programs are described in section 6.5.

The TB486 allows the Flash File System to access the large Flash chips through a window in the 1M byte address space. Memory management logic in the Elan chip allows the high order address lines of the Flash chip to be changed by software. The Flash File System driver software controls the memory management logic transparently to the user's software.

A ROM disk driver may be available for users who are not using MS-DOS style operating systems. This can be of use for QNX users, for example. A Flash File System for QNX may become available also.

The Flash chip resides on the eight-bit PC/104 data bus.

The BIOS makes use of "shadow RAM" in place of the Flash chip for greater speed. In this scheme the BIOS contained within the Flash chip is copied by the BIOS to DRAM at the same addresses. The Flash chip is then disabled and the BIOS is executed from the 32-bit wide DRAM, much faster than it would be from the Flash chip. Section 6.3 contains further information on BIOS extensions.

2.5 MEMORY ADDRESS MAP

Table 2 shows the memory map as configured by the standard BIOS of the TB486. This table shows the bottom 1M byte address space. Extra DRAM is located immediately above the 1M byte boundary.

Addr	Memory Device Decoded	Size
FFFFF F0000	BIOS in Flash Chip Copied to shadow DRAM during boot sequence	64K
EFFFF E0000	Some of this space is currently used by the BIOS during boot sequence, after which, it becomes free. Available for PC/104 memory mapped boards.	64K
DFFFF D0000	Available for PC/104 memory mapped boards. BIOS Extension code can be located here and optionally shadowed in DRAM.	64K
CFFFF CC000	The Flash File System BIOS extension is initially located here, before it copies itself to low memory	16K
CBFFF CA000	Available for BIOS extension code contained in Flash memory which can be shadowd to DRAM at this address.	16K
C9FFF C0000	Usually the VGA BIOS, which is copied from Flash chip to shadow DRAM at this address. Alternatively used by VGA BIOS on PC/104 bus which can be shadowed.	32K
BFFFF A0000	Usually allocated to VGA memory.	128K
9FFFF 00000	DRAM	640K

TABLE 2 - TB486 ADDRESS MAP - FIRST 1M BYTE

3 PERIPHERALS

This section describes the I/O address map and the on-board peripherals.

3.1 I/O ADDRESS MAP

The TB486 features a number of on-board I/O mapped resources, and supports access to the PC/104 bus I/O space as well.

All I/O mapped functions which are present on the IBM PC/AT are present at the same I/O addresses on the TB486. The TB486 is therefore compatible at the machine code or register level with the IBM PC/AT.

On-board I/O devices include registers within the Elan chip, the Super I/O chip, Ethernet chip and VGA graphics chip. The Super I/O chip contains the floppy and IDE disk controllers, Utility Register, keyboard controller, calendar/clock module and the serial and parallel I/O modules. The on-board I/O addresses are. listed in Table 3.

Those addresses which are not on-board are available for peripheral devices on the PC/104 bus. I/O addressing of PC/104 bus boards is reasonably straight-forward: if an I/O address is not used by on-board resources then it can be allocated to a PC/104 board. Putting this another way, the addresses of PC/104 bus boards should be chosen to avoid the on-board I/O resources.

Note that, in common with many ISA bus I/O boards, address decoding logic on PC/104 boards often decodes only address lines AO - A9, which can result in “aliasing” - whereby a PC/104 board can respond to more than one address. For example, a PC/104 bus board set for I/O address 200h may also respond at I/O addresses 600h, A00h, E00h and so on.

Address	I/O Function
00 - 0F	DMA Controller in Elan
20 - 21	Interrupt Controller in Elan
22 - 23	Elan Chip Setup and Control (CSC) Registers
2E - 2F	Super I/O Chip Configuration Registers
40 - 43	Timer Unit in Elan
60 and 64	Keyboard Controller in Super I/O chip
61	Port B Control/Status Port in Elan
70 - 71	Real Time Clock in Super I/O chip & NMI enable in Elan
80 - 8F	DMA Page Registers in Elan
92	Port A Control/Status Port in Elan
A0 - A1	Interrupt Control/Status Register in Elan
C0 - DE (even addr ONLY)	DMA Controller in Elan
EC - CD	Utility Register in Super I/O chip
EE	Alternate A20 Gate Control in Elan
EF	Alternate CPU Reset Control in Elan
102	Enable Register in 65550
1F0 - 1FF	IDE Disk Controller
2F8 - 2FF	COM2 Serial port in Super I/O chip
300 - 30F	Ethernet Controller Chip
378 - 37A	Parallel Port in Super I/O chip
3B4 - 3B5	Registers in 65550
3BA	Registers in 65550
3C0 - 3DA	Registers in 65550
3E8 - 3EF	COM3 Serial Port in Super I/O chip
3F0 - 3F7	Floppy Disk Controller
3F8 - 3FF	COM1 Serial Port in Super I/O chip

TABLE 3 - ON-BOARD I/O DEVICES

3.2 SUPER I/O CHIP

Many of the peripheral functions are implemented in a single chip, the “Super I/O” chip. This is the PC87306 from national Semiconductor. The following functions are included in the 87306:

- Two serial ports (operating as COM2 and COM3).
- A printer port.
- A keyboard controller (providing a PS/2 mouse as well as the keyboard)
- An IDE disk drive interface.
- A floppy disk controller.
- A real time clock with CMOS SRAM.
- Two 8-bit general purpose I/O ports, used on the TB486 as the “Utility Register’.

Each of these functions (except the general purpose I/O) have their own I/O addresses, allocated at the same locations as in every PC. In addition, the 87306 has its own set of configuration registers, which can be used by the BIOS to enable or disable each function, assign I/O addresses, place the functions in low power modes etc.

3.3 SPEAKER

A PC compatible loudspeaker port is implemented within the Elan. This allows for production of tones, tunes, keyboard clicks etc. PC software which uses the speaker to generate sound will therefore operate as expected with the TB486. The TCDEV has a small loudspeaker mounted to it and connection is made to the TB486 via the J3 I/O cable assembly. External speakers should be connected between the J3 signal called SPKR and VCC (+5V).

(Note that the speaker does not operate in REV B boards. This has been corrected in the REV C design.)

3.4 SERIAL PORTS

The TB486 features three RS-232 serial ports which are accessed as COM1, COM2 and COM3. Additionally the COM2 port can be configured for RS-485 operation.

3.4.1 Signals, Addressing and I.nterrupts

The serial ports are hardware and software compatible with the serial ports used on PCs, and all PC communications software packages should work with the serial ports. The UARTs are 16C550 compatible and thus provide a 16 byte transmit and receive FIFOS.

The COM1 UART is contained in the TB486. The COM2 and COM3 UARTs are contained within the PC87306 Super I/O chip. Note that there are some bugs in the COM1 serial port in the Elan chip, mostly relating to error handling. Thus more complex serial communications software should perhaps be used with COM2 and COM3 rather than COM1. These bugs will be removed in a later release of the Elan. If this is an issue, check with DSP Design.

Connection is made to the COM1 and COM2 serial ports via the 50-way J3 connector. If you are using a TCDEV these serial ports are available through the standard 9 pin D-Type connectors at J4 (COML) and J5 (COM2). These connectors are pin compatible with all PC computers.

Connection is made to the COM3 serial port via the 10-way J7 connector.

The pin assignments of all these serial ports are such that they easily connect to 9-pin D-type connectors. The serial ports provide the full complement of RS-232 signals. Transmit Data, Request To Send (RTS) and Data Terminal Ready (DTR) are outputs from the TB486. Receive Data, Data Carrier Detect (DCD), Data Set Ready (DSR), Clear to Send (CTS) and Ring Indicator (RI) are inputs to the TB486.

Following a reset of the TB486 the serial port are initialized as 2400 baud, one stop bit, eight data bits and no padty. These parameters can be changed by the MS-DOS MODE command.

COM1 serial port uses interrupt level IRQ4 to interrupt the processor. The COM2 serial port uses interrupt level IRQ3. COM3 uses interrupt level IRQ5. Note that in some PC systems with three serial port COM3 shares an interrupt with COM1. The TB486 design allows each serial port to have its own interrupt. (See section 4.5 for information on re-allocating interrupts).

It should be noted that the BIOS does not make use of serial port interrupts, but that most comms software packages enable the interrupts and make use of them to increase the speed of serial data transfer. DSP Design is able to supply an interrupt driven communication package called COMM-DRVDOS - ask for details.

3.4.2 RS-485 Operation

As an option COM2 can be re-configured as an RS-485 serial port. This is done with a solder link on the board - see Appendix B for configuration details.

The COM2 RS-485 port configuration provides either half duplex or full duplex interfaces. In full duplex mode one twisted pair is used for transmission and another twisted pair is used for reception. Full duplex mode would normally be used in point-to- point communication between two computers.

In half duplex mode the transmit and receive twisted pairs are connected together at the TB486. In this mode several boards can be connected to the single twisted pair, with no more than one board driving the cable at once. A suitable protocol needs to be agreed by all nodes on the twisted pair to ensure that only one computer transmits at any one time.

On the TB486 the RS-485 driver is controlled by the RTS bit of the on-board UART. When RTS is off (inactive) the RS-485 transceiver chip does not drive the transmit twisted pair cable. This is the default state after a TB486 reset. When RTS is set active the RS-485 transceiver does drive the transmit twisted pair cable and the TB486 can transmit. Note that the receiver part of the transceiver is always enabled. Thus in half duplex mode COM2 will receive the characters that it transmits itself.

In RS-485 mode the DTR control output has no effect, and the CTS, DCD, DSR and RI status inputs are undefined (they can be in either state, and software must not assume any particular values of these signals).

No RS-485 termination resistors are provided on the TB486. These must be provided externally if required.

When operating as an RS-485 port the COM2 RS-485 signals are re-assigned. Appendix E provides information on RS-485 pin assignments.

3.4.3 Disabling and Powering Down Serial Ports

The serial ports can be individually disabled by the BIOS Setup program (use the Advanced/Integrated Peripherals menu item). When the COM1 serial port is disabled its RS-232 transceiver is also powered down, which can save a small amount of current. When both the COM2 and COM3 serial ports are disabled their RS-232 transceivers are both powered down. See section 6.2 for details of the Setup program.

3.4.4 IRDA Operation

The COM1 serial port can also be configured to operate as an IRDA-compatible infra- red serial comms port. The IRDA standard defines a number of protocols. The TB486 supports the SIR format, with speeds of up to 115k baud. Later Elan chips may support speeds of up to 1.152M baud.

The IRDA transmit and receive data signals are available on the 50-way I/O connector J3 pins 2 and 1 respectively, from where they can be connected to an IRDA infra-red transceiver module. To configure the COM1 serial port as an IRDA port you must use the Advanced/integrated Peripherals menu within the BIOS Setup program (see section 6.2 for details of the Setup program).

• Note that the IRDA pins are accessible on the TCDEV Development System at jumper area El - the transmit signal on El pin 1 0 and, the receive signal on El pin 7. By setting El jumpers to 7 - 8 and 9 - 1 0, and removing other jumpers, the IRDA signals as well as power are available on the mouse connector J8.

3.5 PRINTER PORT

The TB486 implements a full-function Centronics compa tible printer port. This port is the MS-DOS PRN device. The printer port is contained within the PC87306 Super I/O chip.

• The printer port within the Elan chip is not used. The Printer port features an 8-bit data port and the full compliment of control signals - four output signals and five input signals.

The I/O signals on the printer port can be treated as general purpose digital input and output signals, and as such can be used for other applications (such as driving a small LCD display, for example).

• The 8-bit data port is normally used as an output port for driving a printer. Provided that the printer port is set up for bidirectional operation (which it is by default), then it can also be used as an input port. The default setting (after reset) is output. To configure the printer as an input bit 5 of the printer port Control Register must be set to 1. To re-configure as an output set bit 5 to 0. The Control Register is a read/write register located at address 37AH.

The printer port signals are brought out on the 50-way J3 I/O connector on the TB486. On the TCDEV the parallel port is accessed via a PC compatible 25 way female D-type connector.

In some circumstances the parallel port may be able to use interrupt IRQ7 to interrupt the processor. Users should note that the BIOS does not make use of interrupts for accessing the printer port, but other software drivers may do so. See section 4.5 for a discussion of interrupt allocation on the TB486.

The printer port can optionally be configured as an Enhanced Parallel Port (EPP) and as an Extended Capabilities Printer Port (ECP). In EPP mode greater throughput is provided by automatically generating strobe signals. In ECP mode a 16-byte FIFO is provided. Users must provide their own software for these modes. The parallel port mode can be set with the BIOS Setup program (use the Advanced/integrated Peripherals menu item). The port can also be disabled using this Setup program. See section 6.2 for details of the Setup program.

3.6 CALENDAR CLOCK CHIP

Calendar/Clock facilities are provided in PC computers. The calendar/clock module is often known as the Real Time Clock, or RTC. These RTC functions emulate those found in the Motorola MC146818 chip, and include time of day functions, calendar functions and CMOS RAM for storing setup parameters. An alarm facility is also provided; this allows an interrupt to be generated when a particular time is reached.

Calendar/clock functions are implemented within the Elan chip and within the 87306 Super I/O chip. However, because of a bug in the Elan calendar/clock the TB486 design uses the 87306 calendar/clock. The calendar/clock chip may be accessed through the MS-DOS calls (interrupt 1AH) or with MS-DOS TIME and DATE commands. As well as the calendar clock functions there are 242 bytes of static RAM which are backed up by the battery. This is used to store configuration parameters used by the BIOS. The serial EEPROM can be used to store these parameters in systems which have no battery - see section 6.7 for details.

A battery can be used to provide power to maintain the clock and CMOS RAM when the main +5V power supply is not present. This external battery should be connected between the BATT input and GND of J3. The battery voltage should be between 3.0V and 3.6V and can be either be a rechargeable battery (e.g. Nicad) or a non- rechargeable battery (e.g. Lithium).

The Elan chip draws approximately 22uA from the battery when the TB486 is powered down and draws no current when operating normally (i.e. powered up). Note that if the battery voltage is higher than about 4V the battery will be supplying current even when the TB486 is powered on.
The TCDEV has a 3.6V l00mAhr Nicad rechargeable battery installed. This connects to the BATT input via an enable/disable jumper, as described in the TCDEV manual. It is estimated that the TCDEV Nicad battery should be sufficient for the clock to operate for several months in the absence of the +5V power supply. The jumper E2 is provided on the TCDEV which can be used to disconnect the battery in order to extend the battery life. The battery should be disconnected while the TB486/TCDEV is in storage.

Figure 2 gives a suitable circuit for a rechargeable battery back-up circuit. NOTE: The circuit shown above is identical to the circuit used on the TCDEV. This circuit is suitable only when using a Nicad battery of the type used on the TCDEV. The circuit shown in figure 2 is ***not*** suitable for Lithium or other battery types. Diode D1 and the resistor must be omitted if a lithium battery is used.

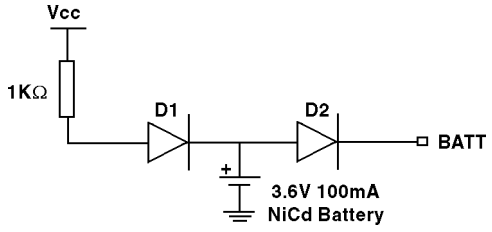

FIGURE 2 - RECOMMENDED BATTERY BACK-UP CIRCUIT

3.7 FLOPPY DISK DRIVE

The TB486 includes an on-board floppy disk controller. The floppy disk controller electronics are included within the Super I/O chip.

Due to a limitation on PCB space the floppy disk controller is accessed through a 26- way flat flexible cable connector, J6, rather than the more common 34-way IDC connector. The 26-way connector is used on floppy disk drives used in laptop PCs. The cable carries power as well as control and data signals. The laptop floppy drives tend to be much smaller than the drives used in desktop PCs. The signals used on the flat flexible cable are the same as used on the 34-way connector, so if necessary the more common floppy drives could be driven.

DSP Design is able to supply suitable floppy disk drives and the 26-way cable assembly.

The TCDEV development system incorporates a complete floppy system, including a floppy diskette drive and cable. The TCDEV also provides an IDE disk controller. Connection to the TB486 is via the PC/104 bus.

Users will probably prefer to use these TCDEV floppy and IDE controllers while using the TCDEV. To do this the TCDEV controllers must be enabled at jumper area E4 and E5. In addition, the floppy and IDE disk controllers on the TB486 must be disabled. This is achieved using the Setup program. The TB486 on-board floppy and [DE disk controllers are controlled through the Advanced/integrated Peripherals menu.

The floppy disk circuit uses an interrupt and a DMA channel. These can be re-assigned to other uses if the floppy disk controller is not used

3.8 IDE DISK DRIVE

The TB486 includes an on-board IDE disk controller. The IDE disk controller electronics is included partly within the Super I/O chip and partly within the disk drive itself.

IDE disk drives can be connected through the 44-pin 2mm pitch connector, J5. One or two drives can be connected on this cable - one configured as a master and the other as a slave. Two hard disks or one hard disk and one CD-ROM drive can be connected.

DSP Design also manufacture a solid-state IDE disk drive which uses Compact Flash memory modules. This is the CF100 product.

The TB486 BIOS can identify the drive type and its parameters. This is done in the BIOS Setup program. Use the Main/IDE Adapter 0 Master menu item. The parameters should then be saved.

A 2½ inch to 3½ inch IDE drive converter cable is available which allows 3½ inch hard disk drives to be connected to the TB486 (a separate power source is required for the 3½ inch drive in this configuration). The converter cable is called the IDE3020.

The TCDEV development system also incorporates an IDE disk controller, as well as a floppy disk controller and drive. Connection to the TB486 is via the PC/104 bus. The TCDEV also uses a 44-way 2mm connector to connect to the IDE drives.

Users will probably prefer to use these TCDEV floppy and IDE controllers while using the TCDEV. To do this the TCDEV controllers must be enabled at jumper area E4 and E5. In addition, the floppy and IDE disk controllers on the TB486 must be disabled. This is achieved using the Setup program. The TB486 on-board floppy and IDE disk controllers are controlled through the Advanced/Integrated Peripherals menu.

The CF100 solid-state IDE disk drive is a small printed circuit board which contains a connector for a Compact Flash memory module. The removable Compact Flash modules are available in a wide range of sizes from 2M bytes to 48M bytes and beyond. The CF100 PCB can be fixed to the TB486, mating directly on the J5 IDE connector. Alternatively it can be connected to J5 through a length of ribbon cable, and thus mounted elsewhere on the TB486 or elsewhere within the TB486's enclosure.

3.9 VGA GRAPHICS

The TB486 provides a powerful VGA graphics system. The VGA controller chip is able to support CRT displays and most types of flat panels including mono LCDS, passive STN and active-matrix TFT colour LCDS, EL and plasma panels. The CRT and flat panel can operate simultaneously.

On the TB486 a Chips and Technologies 65550 VGA controller chip is fifted, together with 2M byte of video RAM. This provides for resolutions of up to 1600 x 1280 and up to 24 bits per pixel, in most combinations. (The product of the number of pixels and the number of bytes per pixel must be less than 2M bytes).

•The VGA controller chip is connected to the processor local bus (the VL bus), and data transferred to and from the VGA memory is thus much faster than in ISA bus systems.

•Connection to a CRT from the TB486 is made via the 16-way connector J9.

Connection to flat panel displays is made through the 40-way 0.05" pitch connector J10. Connection is made from the J10 connector to flat panels using a ribbon cable.

DSP Design also makes a range of interface boards for the display end of this 40-way cable. These interface boards suit many TFT LCD displays, from 640 x 480 up to 1024 x 768 pixels. The interface boards, known as the TFTIF range, solve the otherwise tedious problem of wiring between the TB486 and the display. These interface boards carry power to the displays from the TB486, and can switch off power to the LCD when the display is placed into a suspend mode. The interface boards also convey a backlight enable signal from the TB486 to the display, from where it can be taken to the backlight inverter. Appendix F contains descriptions and pin assignments of these interface boards. See Appendix D for ordering information.

Most flat panels will connect directly to the TB486 through the signals provided on J 1 0. Mono LCDs however, and some colour LCDS, require a Vee supply voltage, typically about -20V. This Vee is not provided by the TB486, and users will have to provide their own Vee if required. The falling prices of colour TFT displays (which do not require Vee) are likely to make mono LCDs less attractive to most users.

The TB486 drives the flat panel signals at 3.3V levels, rather than 5V levels. These 3.3V signals are compatible with both 5V and 3.3V displays. The 40-way ribbon cable carries both 5V and 3.3V power supplies to the flat panel display.

The BIOS searches for VGA boards on the PC/104 bus. If these boards are located then the 65550 and VL bus are disabled and the off-board VGA board is used instead. The on-board 65550 VGA controller chip can be disabled completely, if necessary, allowing an alternative PC/104 VGA controller board to be used. This is done by the BIOS Setup program.

The standard VGA BIOS installed on the TB486 drives a 640 x 480 TFT LCD simultaneously with a CRT. If the CRT is not plugged in when the TB486 is reset then the CRT interface circuitry in the 65550 is switched off to save power.

A number of alternative VGA BIOSes are provided for the 65550 chip. One is already installed in the Flash memory chip on the TB486, and further VGA BIOSes are provided on the TB486 Utilities Disk. The 65550 can drive CRT only, flat panels only, or simultaneous CRT and flat panel displays. The 65550 can also determine whether a CRT is connected, and can turn off the analog CRT circuitry to save power if the CRT is not connected; this is the default on the TB486 VGA BIOSes.

•Many types of flat panels can be driven, and different variations of BIOS are required depending on the display type. The Utilities Disk contains a number of pre-configured VGA BIOSes, and a program which allows further customization of the VGA BIOS. See the README.TXT file on the EC586 Utilities Disk for details. Also present are a number of VGA debugging and utility programs which may be of use, as well as information on the 65550 chip and its BIOS.

Drivers for Windows operating systems (Win 3.lx, Win 95 and Win NT4.0) are also provided on the TB486 Utilities Disks. These drivers will provide higher speed graphics operation than using the standard Windows VGA drivers. Note that at the time of writing the Chips and Technologies drivers cannot be used if power saving is in use, or if the CPOU clock frequency is set to 16MHz or below. We are investigating this problem and will attempt to fix it.

3.10 KEYBOARD AND MOUSE

The TB486 uses an AT type keyboard. Your supplier can provide a suitable keyboard.

In many applications the familiar desktop keyboard is inappropriate. A variety of industrial keyboards and keypads are available - contact your dealer or DSP Design for details. The TB486 will work without a keyboard if required.

Users should avoid plugging in the keyboard or mouse when the TB486 is powered on. The keyboard controller circuitry on the TB486 is contained within the Super I/O chip, and also includes a PS/2 style mouse port. The keyboard uses the IRQL interrupt line and the mouse uses IRQ12. Connections to the keyboard and mouse are made through the 50-way J3 connector. If you are using the TCDEV the keyboard and mouse are accessible through the J8 mouse port connector (PS/2 style) and the J7 AT keyboard connector.

3.11 SERIAL EEPROM

The TB486 has a serial EEPROM chip fifted. This is used primarily to store set-up parameters in systems which lack a battery to retain configuration data in the CMOS RAM. There is some space available in the serial EEPROM for users'data. The serial EEPROM chip also contains the watchdog timer, which is also accessed through the EEPROM's serial interface.

See section 6.7 and 6.8 for information on using the serial EEPROM utility programs. See section 5.2 for details of the watchdog timer.

3.12 ETHERNET

The TB486 includes a 10Base-T Ethernet controller chip. This allows the TB486 to form part of a Local Area Network (LAN).

The chip is the Crystal Semiconductor CS8900. It is I/O mapped and uses one interrupt. Drivers are available for a number of operating systems, including DOS and Windows. These are found on the TB486 Utilities Disks. Drivers for other operating systems, such as QNX and Win'CE may also be available. Contact DSP Design for details. Also on the Utilities Disks is a configuration and test program.

The Ethernet chip is connected to the twisted pair cable through a small printed circuit board called the TB486ET. This is joined to the TB486 with a short length of unshielded twisted pair cable. The TB486ET contains the Ethernet isolation transformer, EMC filters and an RJ45 connector with status LEDs. The TB486ET is designed to be mounted on the enclosure; this location allows EMC filtering to be optimised.

The TB486ET has two status LEDs. The green LED connects to the LINKLED pin of the CS8900 and glows whenever the CS8900 receives valid 10Base-T link pulses. The Yellow LED connects to the LANLED pin of the CS8900 and glows when the CS8900 transmits or receives a frame, or when it detects a collision.

A serial EEPROM is connected to the CS8900. The EEPROM is programmed during the manufacturing process. It contains the 6-byte Ethernet address (IA, or Individual Address), as well as defining the I/O address of the Ethernet board and other parameters.

3.13 ANALOG TO DIGITAL CONVERTER

The TB486 includes a four channel 12-bit analog to digital converter chip. The converter allows analog signals to be monitored.

The analog to digital converter is a Maxim MAX1247 device. Communication with the A/D chip is through a serial link which is implemented in the Utility Register. Using this communications link the processor may configure the A/D converter, place it in a low power mode, or make conversions.

• The A/D converter has four inputs, called ADCO, ADC1, ADC2 and ADC3. These inputs can be between OV and +5V. The input voltages must not extend beyond this range, or else internal protection diodes will begin conducting. If there is a chance of the supply voltages exceeding the supply rails then current limiting resistors must be added external to the TB486, to limit this current to 4mA. This same restriction applies when the power is switched off - if the analog voltage is still applied to the A/D chip when the TB486 is powered off then the internal protection diodes will conduct, and so the current limiting resistors must be used.

•The voltages are measured as a proportion of a reference voltage, VREF. VREF defines the input voltage which provides the full-scale digital reading. The VREF pin on the A/D chip can be driven from an external voltage source, or from the on-board VCC supply voltage. A solder link allows this selection to be made. The accuracy of the measurement of course will be limited by the accuracy of the VREF voltage.

Measurements can be made as “single-ended” or “differential” measurements, as programmable options. In single-ended mode each of the four inputs are measured with respect to the AGND (OV) pin. (AGND is connected to the digital GND at a single point on the TB486). In differential mode the difference between two inputs is measured. The difference between ADCO and ADC1 can be measured, as can the difference between ADC2 and ADC3.

Measurements can also be made as unipolar or bipolar, as programmable options. In Unipolar mode an input voltage of AGND will give a digital output of 0000h, and an input voltage of VREF will give a digital output of OFFFH. In bipolar mode an input voltage of VREF/2 will give a digital output of 0000h, an input voltage of VREF will give a digital output of 07FFh, and an input voltage of OV will give a digital output of 800h. Voltages between 0V and VREF/2 are treated as negative voltages, and converted into twos complement negative numbers. It is probably only sensible to use bipolar mode in conjunction with differential mode, where the difference between two inputs can be negative as well as positive.

Sample software for the A/D converter is provided on the TB486 Utilities Disk. This software makes measurements using the A/D converter. The software may be used as a guide to users who wish to write their own A/D code.

A temperature sensor is provided on the TB486. This is mounted close to the Elan chip, and thus measures a temperature which will be close to that of the Elan package. Thus the temperature of the Elan Gan be estimated. This feature was added to allow the power management software to slow the processor down if it got too hot. At the time of writing this power management feature has not been implemented.

The temperature sensor is connected via a solder link to ADC3. If ADC3 is required to measure an off-board voltage then the solder link can be removed.

The temperature sensor is the National Semiconductor LM60C. It has a voltage output given by:

V = (T x 0.00625) + 0.424

where T is temperature in degrees C.

Expressed differently, the output is 6.25mV per degree C, with an offset such that 0 degrees C gives 424mV. Alternatively: T = (V - 0.424) x 160 The data sheets for the MAX1247 and the LM60C are on the TB486 Utility Disks.

3.14 UTILITY REGISTER

The TB486 has a Utility Register which controls a number of peripheral functions including the serial EEPROM, analog to digital converter interface and power management. The Utility Register is located within the PC87306 Super I/O chip and appears in the I/O address space. The Utility Register occupies two 8-bit I/O locations at addresses OECh - OEDh.

•The Utility Register is used extensively by power management code, the Flash File System driver software and the serial EEPROM software, and will not normally be accessed by the user.

Table 4 gives the function of each bit in the Utility Register. Note that this is for REV C version of the TB486. The REV B board has some differences.

Following reset all bits are set to logic 1. They have internal pull-up resistors fifted, and can be set to 0 by writing a 0 to the Utility Register or by an external device (e.g. the serial EEPROM) pulling a pin to 0. The registers are read-write. When writing to the registers the user should read the current state, change only the required bits, and write the results back (with one exception, noted in the table). Users should not change bits they do not understand, or the TB486 may stop working.

Port	Bit	Signal	Function
ECh	0	BA21	For Flash memory bank switching.
	1	Not Used	
	2	/ENFLASH	Enables access to the Flash memory chip when 0.
	3	/CSADC	To CS pin of the A/D converter. Active low.
	4	/CSEEPROM	To serial EEPROM. Active low.
	5	SK	Clock to serial EEPROM. Active low.
	6	SI	Data to serial EEPROM and A/D converter.
	7	SO	Data from serial EEPRO.M and A/D converter. (always write this bit as a 1)
EDh	0	COMMOFF0	Com1 RS-232 transceiver off when logic 1.
	1	COMMOFF12	Com3 and Com3 RS-232 transceivers off when logic 1.
	2	ETHEROFF	To Ethernet chip. Chip off when logic 1.
	3	/VGAOFF	To 65550 chip. Chip off when logic 0.
	4	CLOCKOFF	Disables clock circuitry. Clock is off when logic 1.
	5	ADCOFF	Disables the A/D converter. Off whoc logic 0.
	6	/32KEN	Routes 32KHz clock to 65550. Enabled when logic 0.
	7	BA20	For Flash memory bank switching.

TABLE 4 - UTILITY REGISTER BIT ALLOCATIONS

4 PC/104 BUS AND STAND-ALONE OPERATION

The TB486 will operate as a stand-alone single board computer, or it can use the PC/104 bus interface to expand its capabilities with the wide range of PC/104 bus I/O cards currently available. This section of the manual describes first the stand alone operation and then operation on the PC/104 bus.

4.1 STAND-ALONE OPERATION

The TB486 will operate as a single board computer with the addition of the appropriate peripherals and a single +5V power supply. In stand-alone operation the TB486 need not be plugged into a bus.

The TB486 requires a +5V power supply. Power can be supplied in one of three ways.

The best option is to use the power connector J4. This is a four pin right-angle Molex socket. Appendix E includes pin assignments of this connector and part numbers of suitable mating connector. The second option is to use the PC/104 bus. The PC/104 bus connectors include a number of +5V and GND pins. Some or all of these pins can be connected in parallel and the resulting +5V and GND connected to the power supply. The third option is to provide power to the board through the 50-way I/O connector J3. This also includes a number of +5V and GND pins.

Users should take care to provide power to the TB486 through cables which are as short and thick as possible, and to make use of as many of the power and ground pins as possible, connecting them in parallel. This is to minimise the voltage drop which will occur through the resistance of the power cables.

4.2 PC/104 BUS

The PC/104 bus is the same from an electrical and timing point of view as the ISA bus found in PC computers. However it is mechanically different, using a stacking connector instead of the gold-plated edge connector used in the PC.

The PC/104 interface is via the Jl and J2 connectors along the bottom edge of the TB486. The 64-way Jl connector provides the 8-bit data bus and the 40-way J2 connector provides the 16-bit signals. The TB486 is able to interface with both the 8-bit and 16-bit modules that meet the PC/104 specification.

The TB486 is PC/104 compliant. That is, the TB486 conforms to both the electrical and mechanical specifications laid down by the PC/104 V2.3 document. There are some minor limitations on TB486 PC/104 bus operation, which are discussed below.

The TB486 complies with the mechanical aspects of the PC/104 V2.3 specification. This includes the use of polarizing pins on the Jl and J2 connectors. Some earlier versions of the PC/104 specification did not use polarizing pins and it was seen that this could result in possible misalignment and subsequent product failure if power was applied before the error was discovered. “Key” positions have been assigned to the Jl and J2 connectors. These can be seen on the Jl and J2 pin assignment diagrams detailed in Appendix E. The key positions have had their pin removed and the socket hole has been blocked to prevent entry by any adjacent pin.

Users should note that any boards produced to, PC/104 specifications prior to V2.2 might not mate with V2.2 or V2.3 boards. Prior to the V2.2 specification the key positions were not present, and J2 could optionally have been a right-angled connector. The V2.2 and V2.3 specifications do not allow the right-angled J2 connector. Both the Jl and J2 connectors on the TB486 are mounted vertically.

•Pull up resistors of 10k ohms have been added to the SD0 - SD15 data bus signals. The IOCHRDY, /IOCS16 and /MEMCS16 signals have 330 ohm pull up resistors. There are pull-up resistors (internal to the Elan chip) on all IRQ signals on the PC/104 bus. The DREQ signals have pull-down resistors (internal to the Elan chip). The /IOCHCHK pins has a pull-up resistor to 3.3V. Note that this pin is not 5V tolerant, so if it is ued it may be pulled to GND but must not be actively driven beyond 3.3V.

As described in section 4.3, the Elan processor does not implement a full ISA bus interface. Some signals are missing or partially implemented. These restrictions are unlikely to cause problems in most circumstances.

4.3 PC/104 BUS LIMITATIONS

The Elan chip does not support a full PC/104 bus interface. The limitations are as follows:

The ZEROWS-, REFRESH- and MASTER- signals are not provided. The Elan does not have a dedicated NMI pin, but a number of general purpose pins may be programmed to generate NMIS. The Elan signal called ACIN has been routed to the PC/104 bus NMI signal (called IOCHCHK- on Jl), and a resistor added to pull this up to 3.3V. At the time of writing the BIOS has not been changed to support this signal as a NMI. Contact DSP Design if you need a non-maskable interrupt.

The two clocks BUSCLK (running typically at 8MHz and in sync with the bus timing signals) and OSC (a free running 14.318MHz signal sometimes used as a reference) are not provided by the Elan. DSP Design have added extra circuitry to provide both of these, though BUSCLK will be running asynchronously with respect to the bus cycles. Section 4.4 contains more information on clocks.

The SMEMR- and SMEMW- signals are not provided by the Elan. These two signals are active on the ISA bus only during accesses to the bottom 1 M byte of the address spare. The MEMR- and MEMW- signals, which are active during all memory read and write cycles, are generated by the Elan. In the TB486 design the MEMR- and MEMW- signals are sent to the SMEMR- and SMEMW- pins as well.

Although the Elan includes a full interrupt controller internally, only eight interrupt request pins are provided on the Elan package. The eight physical pins can be allocated by software to any of the 15 interrupt channels supported by

the internal interrupt controller logic. In practice, the BIOS programs all eight pins to on-board resources which require interrupts. These pins are also connected to the PC/104 bus, where they can be accessed if the on-board resource is not using the signals. Section 4.5 includes more information on interrupts.

Although the Elan includes a full DMA controller internally, only two DMA channels are provided with pins on the Elan package. That is, there are two physical DMA channels external to the Elan, each with a DMA request pin and a DMA acknowledge pin. These two pairs of pins can be allocated to any of the seven channels found on the ISA bus, under software control. Section 4.6 contains more information on DMA.

4.4 PC/104 CLOCK AND RESET SIGNALS

Two PC/104 clocks are provided: the bus clock (BUSCLK) and an oscillator (OSC). The BUSCLK runs at 8.0MHz. The OSC signal is a clock running at 14.3181 MHz.

In most ISA bus computers the bus data transfer cycles are synchronised with the BUSCLK clock. The Elan's internal ISA clock is not brought out of the chip to be used as BUSCLK, so in the TB486 design DSP Design have provided a free-running 8.0MHz Clock for BUSCLK. This clock is not synchronised to the PC/104 bus cycles. This is unlikely to be a problem for most users, since only very few ISA bus peripherals will require the BUSCLK signal at all, let alone a clock which is synchronised with the ISA bus cycle.

Both OSC and BUSCLK can be turned off under software control. See section 7.3 for details.

The TB486 can reset the PC/104 bus. See section 5 for details. The TB486 drives the PC bus RESETDRV signal but cannot be reset by the RESETDRV signal. The TB486 can be reset by issuing a low going pulse on the /RESET line of the J3 connector. In this way a system reset can be generated by an external signal or switch. The TB486 will then force the RESETDRV signal of the PC/104 bus to be driven. The TCDEV has a push button switch connected between /RESET and GND. Pressing this switch momentarily will reset the system.

The Elan processor itself contains two registers which can be used to force a reset of the Elan processor. These are at I/O addresses 92h and EFh. The port 92h register is common to most PC compatible computers. The port EFh register however is unique to the Elan. Reading from port EFh will force the processor to reset. Users must therefore avoid reading from this address.

Neither of the internal reset ports will cause the RESETDRV signal to be asserted, nor will any of the on-board peripherals receive a physical reset.

4.5 INTERRUPTS

The Elan processor contains the same interrupt controller circuit as is present on all PC computers. This consists of two 8259 type interrupt circuits, each with eight interrupt inputs. One 8259 is connected in cascade with the other, leaving 15 interrupts available.

Some of these fifteen interrupts can be used internally to the Elan chip for functions such as the timer interrupt and serial port interrupt. Due to a lack of pins on the Elan chip, only eight interrupt signals are brought out of the chip to be connected to peripherals on the TB486 and on the PC/104 bus. However, so as to provide the greatest flexibility, these eight interrupt request pins are programmable. That is, each of the eight interrupt pins can be programmed to be routed to any of the fifteen normal PC interrupts.

Even so, due to the number of devices on the TB486 which are able to generate interrupts, there may not be many interrupts available for use by other PC/104 boards. To give the users the greatest flexibility, the interrupt pins are mostly routed to an on- board device capable of generating an interrupt (such as the Ethernet chip for example) and also to the PC/104 bus. If the on-board device is not using the interrupt then it can be disabled and its interrupt can be used by another board on the PC/104 bus.
Table 5 shows how the interrupts are assigned. The fifteen entries in the table are the 11 usual" PC interrupts. The next column is either marked "internal", indicating that the interrupt is routed entirely within the Elan chip, or else indicates which one of the eight programmable pins is normally used to provide external access to that interrupt.

* Note - PIRQ5 can be connected to either of these sources by a solder link.

PC IRQ	Internal, External	Allocation
0	Internal	Timer
1	PIRQ1	Keyboard in 87306 Super I/O chip
2	Internal	Cascades second 8259 chip
3	PIRQ3	Com2 in 87306 Super I/O chip
4	Internal	Com1 in Elan chip
5	PIRQ0	Com3 in 87306 Super I/O chip
6	PIRQ6	Floppy disk drive in 87306 Super I/O chip
7	PIRQ5 *	Printer port in 87306 Super I/O chip
8	PIRQ5 *	Alarm interrupt from RTC in 87306 Super I/O chip
9	Not Used	
10	PIRQ4	Ethernet
11	Not Used	
12	PIRQ2	Mouse in 87306 Super I/O chip
13	Not Used	
14	PIRQ7	IDE disk drive
15	Not Used	

* Note: PIRQ5 connected to either of these sources by a solder link.

TABLE 5 - INTERRUPT ALLOCATION

Note that the serial ports and printer have individual interrupt enable bits, within their register sets. The default is for these interrupts to be disabled. This means that IRQ4, IRQ5 and IRQ,7 can be used by other PC/104 boards if the interrupts are not being used by the COM2, COM3 and printer ports.

It may be possible to add a non-maskable interrupt to the Elan. The Elan does not have a dedicated NMI pin, but a number of general purpose pins may be programmed to generate NMIS. The Elan signal called ACIN has been routed to the PC/104 bus NMI signal (called IOCHCHK- on JI), and a resistor added to pull this up to 3.3V. At the time of writing the BIOS has not been changed to support this signal as a NMI. Contact DSP Design if you need a non-maskable interrupt.

Note that the ACIN pin is not 5V tolerant. This means if you are driving the /IOCHCHK pin you may pull it to GND, but must not drive it actively high beyond +3.3V.

The /IOCHCHK is an active-low interrupt. All the maskable interrupts are programmed to generate an interrupt on a positive-going edge.

4.6 DMA

The Elan processor contains the same DMA controller circuit as is present on all PC computers. This consists of two 8237 type interrupt circuits, each with four DMA Request (DREQ) inputs and four DMA acknowledge (DACK) outputs. One 8237 is connected in cascade with the other, leaving seven DMA channels available.

Although the Elan includes a full DMA controller internally, only two DMA channels are provided with pins on the Elan package. That is, there are two physical DMA channels external to the Elan, each with a DREQ pin and a DACK pin. These two pairs of pins can be allocated to any of the seven channels found on the ISA bus, under software control.

One pair of DMA pins (PDRQO and /PDACKO) is normally programmed by the BIOS to be DMA channel 2, and is connected to the on-board floppy disk controller, as well as to DREQ and /DACK pins on the PC/104 bus. If the floppy disk controller is disabled then these pins can be used for DMA devices on the PC/104 bus.

The other pair of DMA pins (PDRQL and /PDACK1) is connected to DREQ and /DACK pins on the PC/104 bus.

To provide maximum flexibility for users with PC/104 boards which use DMA, the Elan's DMA signals are connected to several places on the PC/104 bus connectors.

The PDRQO and /PDACKO signals are connected to the Jl connector in the DMA channel 2 position, and also on the J2 connector in the DMA channel 0 and channel 7 positions. Obviously only one of these three channels can be used at any one time. The selection is made by an option in the Setup program.

•The PDRQL and /PDACK1 signals are connected to the Jl connector in the DMA channel 1 position, and also on the J2 connector in the DMA channel 5 position. Obviously only one of these two channels can be used at any one time. The selection is made by an option in the Setup program. (This pair is also connected to the DMA pins on the Ethernet chip, although DMA is not normally used by the Ethernet drivers).

DMA channels 0, 1 and 2 can be used for 8-bit DMA transfers, and DMA channels 5 and 7 can be used for 16-bit DMA transfers. Thus the options provided should allow users to have two 8-bit channels in operation, or two 16-bit channels, or one of each.

5 HARDWARE RESET OPTIONS

A full set of hardware reset options exist for the TB486. The reset circuit is built around the X25043 serial EEPROM chip, which provides reset functions as well as memory. This chip includes a power supply monitor and a watchdog timer. To avoid glitches on the reset signal the X25043 will always hold the reset signal asserted for approximately 200ms. This ensures all circuitry is properly reset, and conforms to the PC/104 bus specification.

The X25043 resets the Elan chip, and on-board circuitry. The Elan responds to its reset by driving the RESETDRV signal high.

5.1 POWER SUPPLY MONITOR

The X25043 monitors the +5V supply voltage. When the supply drops below about 4.5V the X25043 will assert the TB486 reset signal. Once the power supply returns to within specification, the reset signal will be released after further 200ms. This circuit prevents power "brown-out" causing unpredictable behavior.

Users should note that if the voltage drop across the cables which link the power supply to the TB486 is excessive then the power supply monitor may reset the TB486. This may also happen if there are noise spikes on the power supply. It is recommended that all power supply cables be as thick and short as possible to minimize the voltage drop across them.

5.2 ONBOARD WATCHDOG TIMER

A watchdog timer exists on the X25043. The function of a watchdog'timer is to reset a computer if the software has crashed. The correct operation of the timer relies on software to access the watchdog timer hardware on a regular basis. If the software crashes, the watchdog timer will not be "kicked" and so eventually it will time-out and reset the computer. The watchdog timer function is accessed via the Utility Register.

The Utility Register is a multi-function register which among other things gives access to the four control signals on the X25043 serial EEPROM. The Utility Register is described in section 3.12. The watchdog is enabled by writing an enable command to the X25043 via the Utility Register. Once this has been initiated, an internal clock to the X25043 starts counting and will continue to count until it times out, until the watchdog timer is "kicked" by the user's application software, or until the watchdog timer is disabled by a disable command sent to the X25043.
The watchdog timer period can be set to approximately 1.4s, 600ms or 200ms, or it can be disabled, by writing different command words to the serial EEPROM command register. Once it has been enabled the watchdog timer must be accessed repeatedly by the user's software. If the watchdog timer is allowed to time out the X25043 chip will issue a hardware reset to the TB486 (and to the PC/104 bus).

The watchdog timer is “kicked” by taking its chip select (/CS) pin low then high. The /CS pin is driven by bit 4 of the Utility Register at I/O address OECH. The TB486 Utility Disk has documented sample code illustrating the use of the watchdog function, and also includes the data sheet of the X25043. Note that it is the responsibility of the user to design code which will reliably kick the watchdog timer. The BIOS includes code which disables the watchdog timer immediately after a reset, and thus if a watchdog time-out occurs the watchdog timer is disabled until after the operating system is loaded and the application software re-enables it. See section 6.7 for further information on the watchdog timer. The watchdog timer is disabled prior to entering Standby or Suspend modes. After resuming operation the watchdog timer is restored to its previous state.

5.3 RESET SWITCH

The TB486 can be reset by issuing a low going pulse on the /RESET line of the J3 connector. In this way a system reset can be generated by an external signal or switch. The reset switch connects between J3 pins 23 and 24. (Pin 24 is the /RESET input, and pin 23 is a GND pin). The TB486 will then force the RESETDRV signal of the PC/104 bus to be driven.

The TCDEV has a push button switch connected between /RESET and GND. Pressing this switch momentarily will reset the system.

5.4 RESETTING THE PC/104 BUS

The TB486 always resets the PC/104 bus via the RESETDRV signal. The active high RESETDRV signal is asserted whenever the X25043 is driving the TB486 on-board reset signal - that is, in response to a power failure, watchdog timer time-out, or a low going pulse on the /RESET line of the J3 I/O connector.

It is not possible to reset the TB486 by driving the RESETDRV signal on the PC/104 bus.

6 SOFTWARE

The TB486 offers a very high degree of PC compatibility. The vast majority of software (both operating systems and applications software) which will run on IBM PC/AT will also run satisfactorily on the TB486.

Most users will wish to use the MS-DOS operating system (booting from a hard disk, floppy disk or Flash File System) and then run off-the-shelf software, or their own application. DSP Design offers a number of software products to ease software development.

6.1 SYSTEM BIOS

The system BIOS is a program which interfaces between the TB486 hardware, the operating system and application code. It is responsible for controlling the TB486 hardware and providing a standard interface to the higher levels of software. The BIOS also deals with functions such as initialisation and testing the TB486 hardware following power-on.

The TB486 uses a system BIOS supplied by Phoenix Technologies. Users should note that the BIOS is the copyright of Phoenix.

The BIOS has an in-built Setup program, which can be invoked by typing the F2 key at the keyboard during the boot sequence. Section 6.2 contains more information on the Setup program.

The BIOS is programmed into the Flash memory chip as part of the manufacturing process. Note that the system BIOS and BIOS extensions are combined in a single 128k byte file, which is programmed into the top 128k bytes of the Flash memory chip. The contents of the Flash memory chip can be changed by the user if necessary, as described in section 6.5. The default is for a system BIOS, a VGA BIOS and the Flash File System BIOS Extension to be programmed into the Flash memory.

A number of pre-configured BIOS files are available on the TB486 Utility Disks. These differ in the BIOS extensions which they contain. See the README.TXT file in the BIOS directory of the TB486 Utility Disks for further details.

Under some circumstances the TB486 BIOS may need to be modified or additional BIOS code may need to be added to the BIOS EPROM. Tools exist to deal with these issues, so contact DSP Design for details.

6.2 BIOS SETUP PROGRAM

The BIOS has an in-built Setup program, which can be invoked by typing the F2 key at the keyboard during the boot sequence. The setup program allows many system parameters to be changed, and then stored in CMOS memory. Amongst the parameters which can be changed are the current time and date, disk drive types, enabling and disabling peripheral devices, security and power management.

The Setup progarm is menu driven, and its operation should be self-explanatory. Users must not change parameters which they do not understand.

A number of default settings will be loaded the first time the TB486 is re-booted after a CMOS battery backup failure. This will load in the default values suitable for operation with the TCDEV Development System. The default values can also be restored by an option in the Setup program's Exit menu. In addition, the F9 key can also be used to reset only those settings on the currently displayed Setup menu. The Serial EEPROM can be used to store CMOS SRAM contents - see section 6.7 for details.

Many on-board peripheral devices can be enabled or disabled by the Setup program, in the Advanced/integrated Peripherals menu. When peripherals are disabled they are placed into a low power mode, and their I/O addresses and interrupt signals become available for other PC/104 boards. This could be required, for example, to allow the TB486 to co-exist with other PC/104 boards which are already using the standard COM1, COM2 and PRN I/O addresses.

The IDE and floppy disk controllers are amongst those devices which can be enabled and disabled using the Setup program. If the floppy and IDE disk controllers on the TCDEV development system are to be used then the on-board controllers must be disabled. If the on-board floppy and IDE controllers are to be used then they must be enabled using the Setup program. The default is for the on-board disk controllers to be to be disabled, to facilitate use of the TCDEV Development System.

Do not attempt to use one on-board disk controller and one off-board disk controller.

The Setup program allows hard disk drive parameters to be defined. The "Auto-type Fixed Disk" option will usually be the best way of setting the IDE disk drive parameters. If the floppy and IDE controllers are changed from disabled to enabled then a re-boot is required before the Auto-Type Fixed Disk option can be invoked.

Setup parameters are stored in the on-board CMOS memory, and it is backed-up if an external battery is provided. If no external battery is present then the Setup parameters can be stored in an on-board serial EEPROM, as described in section 6.7.

The Setup menu includes a security menu. This allows access to the Setup program, floppy disk and hard disk boot sector to be password protected. Care should be taken with this, as if the password is forgotten the battery on the CMOS RAM must be removed to reset the password protection. Worse still (or better still!), if the serial EEPROM is being used to save the CMOS settings in the event of battery failure, the EEPROM will need to be erased or removed before the password protection can be removed.

The Setup program also provides control of the power management features of the TB486. This is described in detail in section 7.

6.3 VGA BIOS AND OTHER BIOS EXTENSIONS

As well as the system BIOS, the Flash memory chip can (and usually does) contain other BIOS extensions. These include the VGA BIOS and the Flash File System BIOS.

6.3.1 PRINCIPLES OF OPERATION

The system BIOS and the BIOS extensions are combined into a single 128k byte file, which is programmed into the Flash memory chip using a Flash programming utility, as described in section 6.5. A number of these pre-configured BIOS image files are present on the TB486 Utilities Disk. The pre-configured files include options with and without the Flash File System driver.

If these pre-configured BIOS image files are not suitable, (for example if other BIOS extensions must be copied into the Flash memory) then a utility program is available for generating new 128k byte BIOS image files. This program is called CRUNCH.EXE, and is provided on the TB486 Utilities Disk. A README.TXT file on the disk describes the operation of this program.

As well as executing BIOS extensions contained within the Flash chip, the BIOS also searches the PC/104 bus for BIOS extension EPROMs which might be present elsewhere in the system. The BIOS searches on every 2k byte boundary from C0000h to just below the system BIOS at F0000h. If valid BIOS extension EPROMs are found on the PC/104 bus then they are executed.

The system BIOS is shadowed, and BIOS extension code in the Flash chip, such as the VGA BIOS and the Flash File System BIOS Extension, are also shadowed. BIOS extensions which may reside on other PC/104 modules (such as VGA boards or LAN boards) may also be shadowed. This shadowing is enabled or disabled by the TB486 Setup program, in the Main/Memory Shadow menu.

Note that if the Flash File System is used then the 64k bytes of memory at address C0000h must be shadowed. Note also that since the Elan chip can only enable shadow memory in 64k byte blocks, if any memory in the 64k byte segment at C0000h is shadowed then all of the 64k byte block will be mapped as shadow RAM. The same applies to the 64k byte segment at D0000h.

6.3.2 THE VGA BIOS EXTENSION

The standard TB486 boards are shipped with a BIOS image which includes two BIOS extensions. One is for the 65550 VGA controller present on the TB486. The VGA BIOS extension is 40k bytes in size, and is located at address C0000h.

The VGA BIOS is optimised for 640 x 480 TFT LCD displays. It will also simultaneously drive a CRT display. However, to save power, if a CRT monitor is not detected at reset time the CRT circuitry in the 65550 will be switched off.

Other VGA BIOS extensions are available on the TB486 Utilities Disk. These are configured for alternative displays. The CRUCH program can be used to remove the default VGA BIOS and replace it with another.

Also on the TB486 Utilities Disk is a program which can be used to customise the VGA BIOS, should it be necessary to do so.

There is a special case relating to VGA BIOS extensions. Before the TB486 BIOS installs a VGA BIOS for the on-board 65550 graphics chip from within the Flash chip it first examines the PC/104 bus, looking for any other VGA BIOS which may be present. If another VGA BIOS exists (because the user is using another VGA controller such as DSP Design's TV750, for instance) then this other VGA BIOS is used and the VGA BIOS in the Flash chip is not used. The on-board graphics sub-system is disabled. This can be a useful feature if more than one VGA board can be used in a system.

6.3.3 THE FLASH FILE SYSTEM BIOS EXTENSION

The standard TB486 boards are shipped with a BIOS image which includes two BIOS extensions. The second BIOS extension is the Flash File System BIOS extension. The FFS BIOS Extension is 16k bytes in size and is located at address CC000h.

The Flash File System device allows the Flash memory to be configured as a disk drive, as described in section 6.6.

The Flash File System is designed for MS-DOS and related operating systems. It is likely that the Flash File System BIOS extension will not operate with some other operating systems, and may need to be removed.

•The Flash File System driver will cause the Windows 95 disk system to run slowly. This is because when the Flash File System is installed Windows 95 uses the 16-bit DOS file system, rather than its faster 32-bit native file system. It is unlikely that Windows 95 users will want to use the Flash File System, so these users should reprogram their Flash memory with a BIOS image without the Flash File System. A suitable BIOS image exists on the TB486 Utilities Disk.

6.4 MS-DOS AND OTHER OPERATING SYSTEMS

The TB486 will run any version of MS-DOS, and should run any other operating system which will run on a PC. The computer will boot MS-DOS from a floppy disk, from a hard disk or from the Flash File System.

DSP Design supply Microsoft's MS-DOS operating system. Bootleg copies of the operating system of course may not be run on the TB486.

Any other operating system which will run on a 386, 486 or Pentium-based desk-top computer should also run on the TB486. For example Windows 3.x, Windows 95, Windows NT and QNX run successfully on the TB486.

Users who are running non-DOS operating systems, including Windows 95, may need to remove the Flash File System BIOS Extension from the BIOS image. See section 6.3.3 for details.

6.5 FLASH MEMORY PROGRAMMING

Flash programming utility programs provide facilities for programming data into the Flash memory chip on the TB486. The programs can erase some or all of the Flash chip, and can write a file from disk to the Flash chip. The most common use of these programs is to safety program the BIOS image file into the Flash memory chip.

The Flash programming utility is normally used to write a new BIOS to the Flash memory. It is not required to create the Flash File System disk in the Flash chip. Care must be taken when using this program to program the Flash chip, since an error can erase the BIOS, which means the TB486 will stop working. Should this happen the TCDEV development system (REV D and later versions only) can be used to restore the contents of the Flash chip. See the TCDEV Technical Reference manual for details.

The following describes the process of programming the AMD or Fujitsu 29F016,chip installed as standard on the TB486. (The default is for 2M bytes of Flash memory; the TB486 can be fitted with 4M bytes as a special order. Boards with 4M bytes will have different instructions - ask DSP Design for details).

The 29F016 flash device is arranged as 32 sectors of 64k bytes each. Each block is erased separately, and it is not possible to erase less than 64k bytes at a time. The TB4FO16.EXE programming utility used to program the 29F016 device is available on the TB486 Utility Disk.

The program can be run two ways - most commonly to safely program a BIOS image file into the Flash chip, and also in a more flexible way, to allow any file to be programmed at any location in the Flash chip.

In the safe BIOS programming mode TB4F016 is run with the following single parameter:

TB4F016 -u<filename> (u for'update BIOS').

Program the specified BIOS image file into the device. In this safe mode the program checks 'to see if the file is present on the disk, and is a plausible BIOS image (i.e. it is 128k bytes in size). The program then erases the top 128k bytes in the Flash memory, and programs and verifies the file.

In the flexible mode TB4F0l6 is run with any or all of the following parameters:

TB4F016 -e -sxx -p<filename> -v<filename> -oxxxxx -lxxxxx -q -dxxxxx -cx -h

-e If -e is specified the entire device will be,.erased. If -e is not specified the device will not be erased. The default is to not erase.

-s If -sxx is specified then the sector specified by xx is erased. The value for xx is a hexa decimal number between 0 and 1F. The BIOS is in sectors 1E and 1F.

-p -p<filename> program the specified file into the device. This parameter defaults to “do not program”.

-v -v<filename> verifies the contents of the flash device against the data in the file specified by <filename>. If the chip and the file differ the address of the first byte which differs is printed, together with the values of the differing bytes. The default is not to verify.

-0 -oxxxxxx. Start programming the file at this offset from the start of the flash device. xxxxxx is a 21 bit (6 hex digit) hexadecimal number. This parameter defaults to 0. For programming the 128k byte BIOS image file you should use the parameter -olE0000.

-l -lxxxxxx. This is the maximum number of bytes of data to program into the Flash chip. The number of bytes programmed will be the either the file length or the number of bytes specified by this parameter, whichever is the smaller. This parameter defaults to the size of the Flash device (200000h bytes in the case of the 29F016).

-q Quiet. This parameter minimizes screen output. The default is “not quiet”.

-d -dxxxxxx. This option displays the contents of the Flash chip at the 21 -bit (6 hex digit) hexadecimal address xxxxxx. The output is 16 lines each of 16 hex bytes. The default is not to print data.

-c -cx. This option allows one or other of the two Flash chips to be selected. The parameter x can be 0 or 1. Flash chip 1 is defined to be the chip containing the BIOS image. This is the chip which is present if only one chip is fifted. The default value is 1.

-h Displays a help menu.

The TB4F016.EXE program can be used to write one or more files to the Flash chip, by running the program several times with different -p, -s and -o options each time.

Once you have re-programmed your system BIOS there are several steps that MUST be undertaken to complete the BIOS update process. These steps are listed below.

1 Re-program the system BIOS as discussed above

2. Re-boot by powering the TB486 system off and on. Do not use a push button reset or a Ctrl-Alt-Del reset.

3. Enter the Setup program by pressing the. F2 key.

4. Once in Setup, make whatever changes are appropriate.

5. If you have a hard disk, ensure you set the correct drive parameters.

6. Save the new settings to CMOS memory and exit. This will cause the TB486 to re-boot using the new BIOS parameters.

7. If you have previously run TB4EE.EXE -C (to save CMOS to EEPROM), then you MUST do this again to save the new BIOS parameters into the serial EEPROM.

6.6 FLASH FILE SYSTEM

This section describes the Flash File System, or FFS. The Flash File system works well with MS-DOS and Windows 3.xx. Users of other operating systems may not be able to use the Flash File System, or may suffer slower disk operation as a result. It may be that a Flash File System may become available for the QNX operating system.

6.6.1 OVERVIEW

The ability to operate without mechanical disk drives is a key feature of the TB486. To do this you can make use of the Flash File System (FFS) which is provided with every TB486. As well as being more robust than mechanical drives they are also faster, at least for read operations.

The FFS provided with the TB486 is the FlashFX product from Datalight Inc. DSP Design have paid a license fee for every standard TB486, so you may use the Flash File System on every standard TB486 you buy. (Some volume users who do not require the FFS may ask for TB486 boards without the license, to reduce costs).

The Flash File System driver is implemented as a BIOS extension or as a loadable device driver. In order to boot the operating system from the Flash File System disk drive the BIOS Extension option must be chosen, as a loadable device driver can only be loaded after DOS has booted from another disk (such as a floppy disk). However, the loadable device driver option can be used when another device (an IDE drive for instance) is the boot device. The loadable device driver is also required during the initial formatting of the Flash disk.

The Flash File System driver is normally implemented as a BIOS extension. This driver must be programmed into the Flash memory, and then it is located every time the TB486 boots. The standard TB486 is shipped with the FFS device driver already present in the Flash memory as a BIOS extension.

The loadable device driver requires the driver to be placed on the boot disk, and it is activated by an appropriate entry in the CONFIG.SYS file.

In normal use you should use either the BIOS extension or the loadable device driver - not both. The only time it is permissible to use both is during initial formatting as explained in section 6.6.2.

In either case, the FFS driver operates by intercepting calls to the BIOS disk drive sub-system, which uses software interrupt INT1 3. Calls which are not intended for the FFS are passed through to the BIOS. Calls which are intended for the FFS are performed by the FFS driver.

The FFS BIOS extension requires 16k bytes of memory, from CC00OH - CFFFFH. A small amount of RAM within the 640k bytes available to MS-DOS is also used by the FFS.

The Flash File System is designed for MS-DOS and related operating systems. It is likely that the Flash File System BIOS extension will not operate with some other operating systems, and may need to be removed.

The Flash File System driver will cause the Windows 95 disk system to run slowly. This is because when the Flash File System is installed Windows 95 uses the 16-bit DOS file system, rather than its faster 32-bit native file system. It is unlikely that Windows 95 users will want to use the Flash File System, so these users should reprogram their Flash memory with a BIOS image without the Flash File System. A suitable BIOS image exists on the TB486 Utilities Disk.

6.6.2 OPERATION OF THE FLASH FILE SYSTEM

The standard TB486 is shipped from DSP Design with the FFS BIOS Extension installed in the Flash memory, and the Flash disk already formatted. Thus most of this section is for information only, as steps 1 - 6 below have already been performed.

The Flash File System software referred to here is on the TB486 Utility Disk, in the FFS directory. To operate with a Flash File System, perform the steps below (these steps assume the default 2M byte Flash chip is fitted. Instructions will be slightly different for the 4M byte chip).

1. Confirm that you have the FFS BIOS extension programmed in the Flash memory along with the system BIOS. If not, suitable BIOS files are present on the TB486 Utility Disk. The standard BIOS includes the FFS BIOS extension.

2 Boot your computer from a floppy disk containing the FFS driver in its loadable device driver form and a suitable entry in the CONFIG.SYS file. The loadable device driver is FTB4F016.SYS and the corresponding entry in CONFIG.SYS is: DEVICE=FTB4FO16.SYS When the Flash File System driver loads it will display a sign-on message to confirm that it has been located.

3 Before the Flash File System can be used the Flash disk must be formatted, using a dedicated formatting program called FXFMT.EXE. The syntax of the FXFMT program is:

FXFMT <drive> /P128 /T<size>M [/options]

<drive> is the drive letter, usually C:
<size> is the size of the flash array to format in Mbytes, usually 2.
[/options] can be any or all of the following:

- /C This is an optional parameter, and tells the program to format the drive without prompting the user for input (not recommended).
- /V This is an optional parameter and allows a volume label to be placed on the disk. After a format, the program will prompt the user for a volume name. Most users will type: FXFMT C: /P128 /T2M

4 At this point you have a functioning Flash disk, although the disk will not be bootable and will have no files on it.

5 Now the DEVICE=FTB4F016.SYS entry should be removed from the CONFIG.SYS file on the boot disk.

6 Once the Flash disk has been formatted the user can use the DOS SYS command to place DOS on the Flash disk. (Note this step is optional, but the operating system must be added if the Flash disk is to be the boot disk). To copy the MS-DOS operating system to the Flash Disk type:

SYS C:

7 At this point the TB486 can be re-booted. If all has gone well the Flash File System BIOS Extension will print a sign-on message and the TB486 will boot DOS from the Flash disk. In a system without hard disk drives the Flash disk will be allocated the drive letter C:, It will be the boot disk (provided that the boot sequence in the Setup utility has C: selected as the boot disk). If IDE drives are included in the system then the Flash disk will be allocated the drive letter following the last IDE drive, and the IDE drive (C:) will be the boot disk.

The FFS implements a wear-leveling algorithm, to ensure that all parts of the Flash chip are equally used.

6.6.3 WRITE OPERATIONS AND GARBAGE COLLECTION

Writes to the Flash disk take longer than reads. This is due to the time taken by the Flash memory chip itself to write data into its memory cells.

When files are deleted the FFS driver does not immediately erase the corresponding Flash memory. Instead, it marks that memory as being “garbage”, and when the Flash memory approaches its capacity the FFS performs a garbage collection process, in which data which is still required is copied into a spare 64k byte block, freeing another block to be erased. The nature of the Flash memory is that it can only be erased in 64k byte blocks. The FFS driver thus has the task of allocating logical disk sectors to physical areas of Flash memory.

As a consequence of the garbage collection process, some writes will take longer than others, if they force the FFS to perform its garbage collection operation. This garbage collection process during Flash writes can increase write time by as much as sixty percent, as the number of garbage areas grow.

The TB486 Utilities Disk contains a garbage collection utility called FXRECLM.EXE. This utility can be used to force the FlashFX FFS to perform a garbage collection operation at any time, when executed. Placing an appropriate entry in autoexec.bat would force garbage collection each time the TB486 boots, helping to keep the flash array performance higher than normal.

FXRECLM.EXE usage:

FXRECLM.EXE <drive> [<count>]

Where
<drive> is the drive letter of the flash disk (e.g. C:), and
<count> is the number of successive garbage collection operations to perform on the flash disk. One garbage collection operation will reclaim one 64k block of flash memory.

The FXRECLM.EXE utility stops the garbage collection process either when <count> has been reached or when there is no more flash memory to recover, whichever comes first.

For 2Mbyte of flash memory there are 32 blocks of 64k bytes each, two of which are reserved for system BIOS use. The remaining 30 blocks are available for flash disk use. Thus to perform garbage collection on all thirty 64Kbyte blocks of flash disk memory use the FXRECLM.EXE utility as follows:

FXRECLM C:30

6.6.4 FLASH FILE SYSTEM STATISTICS

The TB486 Utilities Disk also contains a useful utility for reporting the status of the flash disk. It can be used to find out how much flash memory is available, has been used, and is recoverable through the garbage collection process.

FXINFO.EXE usage:

FXINFO.EXE <drive>

Where
<drive> is the drive letter of the flash disk (e.g. C:)

The FXINFO utility provides a detailed flash disk report, most of which is of little use to TB486 users. However the final ection (an example of which is displayed below), is of use in determining flash memory usage, in particular the ‘Recoverable Space’, information.

The following is an extract from a typical FXINFO display:

...
Media Usage Data Used 944K
Free Space 499K
Recoverable Space 383K

The recoverable space is the amount of memory that can be recovered through the garbage collection process. In the example above the recoverable space is reported at 383Kbytes.

6.7 SAVING CMOS RAM DATA IN THE SERIAL EEPROM

A serial EEPROM chip on the TB486 provides non-volatile memory storage and also incorporates a watchdog timer. The non-volatile memory can be used to back-up the CMOS SRAM, in systems without batteries, or where the battery may go flat. The serial EEPROM chip used is the Xicor X25043. This chip contains 512 bytes of non- volatile serial EEPROM. The serial EEPROM is accessed through the Utility Register in the 87306 chip.

The BIOS includes a feature which checks to see if the contents of the CMOS memory are valid during the boot sequence. If the CMOS memory does not have valid contents (since there was no battery back-up, for instance) then the BIOS will check whether the serial EEPROM contains valid CMOS data. If it does then the data in the serial EEPROM memory will be copied into the CMOS memory and used.

It is the responsibility of the user to program the serial EEPROM. A utility program is provided to do this. It is called TB4EE.EXE and is available on the TB486 Utility Disk. It should be run with the -C parameter, like this:

TB4EE -C

(Note that the TB4EE program has other uses - see 6.8 and 6.9).

The TB4EE program should be run once the CMOS memory contains valid data - after running the BIOS Setup program for instance. The contents of the CMOS registers are then copied into the serial EEPROM. These values will be returned to the CMOS memory by the BIOS if the CMOS memory contains invalid data during subsequent boot operations.

When the TB4EE.EXE program is run all of the first 128 locations in the CMOS SRAM module are copied to the EEPROM. Note the 128 locations are made up of 114 CMOS RAM locations, ten real-time clock time and date registers and four control registers. All 128 are copied to the serial EEPROM. (There are an additional 128 CMOS memory locations which can be accessed when the MEMSEL bit in the 87306 chip is set to logic 1. These locations are not copied to the serial EEPROM.)

During the restore process, when the contents of the serial EEPROM are copied back to the CMOS RAM, all 128 bytes are copied. This restores the time and date, the control registers and the memory locations containing data.

The BIOS only makes use of some of the first 114 CMOS memory locations; the others are available to the users for their own purposes. Bytes from address 62h through to 7Fh are not used by the BIOS. In addition, there are a further 128 bytes available, which can be accessed by setting the RAMSEL bit in the 87306 Super I/O chip to 1. The RAMSEL bit acts as a bank select bit, selecting either the standard 128 bytes or the second 128 bytes. Contact DSP Design if you need to access the second 128 bytes of CMOS SRAM.

Although only 128 locations in the serial EEPROM are currently used by the BIOS to store the CMOS registers, DSP Design strongly recommends that 256 locations in the serial EEPROM up to and including address 0FFh are reserved for possible future BIOS use. This leaves a further 256 bytes in the serial EEPROM (at addresses 100h - 1FFh) available for users. Section 6.8 describes a program which can be used to read and write CMOS EEPROM locations.

6.8 SERIAL EEPROM PROGRAMMING

The X25043 serial EEPROM has 512 (200h) bytes on non-volatile memory. Section 6.7 describes using the serial EEPROM for saving CMOS RAM settings. Addresses 00h - 7Fh in the serial EEPROM are reserved for holding CMOS RAM data, and addresses 80h - FFH are reserved for future DSP Design use. Addresses 1 00h - 1 FFh remain available for users.

The TB4EE.EXE program allows individual bytes in the EEPROM to be written and read. It also provides a way of testing the EEPROM, enabling and testing the watchdog timer, and copying the CMOS SRAM into the EEPROM. It has the following parameters:

-rxxx -r reads the data from the serial EEPROM at the address <xx>, and displays it on the screen. The xxx parameter is a hexadecimal number in the range 0 - 1 FFh.

-wxxx -w writes data into the serial EEPROM at the address defined by the <xx> parameter. The data written is the hexadecimal byte specified by the -d parameter. The xxx parameter is a hexadecimal number in the range 0 - 1FFh.

-dxx -d defines the data value to be written to the serial EEPROM by the -w parameter The xx parameter is a hexadecimal number in the range 0 - FFh.

-t -t tests the serial EEPROM, by writing to every location.

-c -c copies the contents of the CMOS SRAM into the serial EEPROM.

-e -e enables the watchdog timer. The TB486 will be reset unless the watchdog is kicked (see the -k parameter). This is only used for testing purposes.

-kxx -k kicks the watchdog timer for <xx> seconds. The xxx parameter is a hexadecimal number in the range 0 - 1FFh

6.9 WATCHDOG TIMER PROGRAMMING

The watchdog timer is contained within the serial EEPROM chip and is controlled through four pins of the Utility Register. Once it is enabled, the watchdog timer will reset the TB486 if it is not accessed (or “kicked”) regularly. It is up to the user to write code to enable and kick the watchdog timer. As an example, the source code of a watchdog timer test program is included on the TB486 Utility Disk. The test program is called TC5WD.EXE.

The general purpose serial EEPROM program, TB4EE.EXE, can also be used to test the watchdog timer - see section 6.8.

The watchdog timer is kicked by the toggling of its chip select pin (/CS), which is driven by the Utility Register bit 4 at I/O address 0ECH. Users might consider taking the /CS pin low at one point in their program and taking it high again in a different point. This reduces the likelihood that a crashed program could end up executing a small loop which both set and cleared the /CS pin. Similarly, the watchdog accesses should not be part of a timer-based interrupt service routine, since a program could possibly crash and leave a timer interrupt correctly operating.

Care needs to be taken if the TB486 power management is to be used. Power management can slow down the processor clock, or even stop it, so that software loops will execute slowly, or even stop entirely. Thus the possibility exists that watchdog timer would time out.

Consequently, the BIOS disables the watchdog timer before entering Standby or Suspend modes, and re-enables it after resuming high speed operation. Users must be aware of this. In low speed mode the watchdog timer remains operational. Users must confirm that the slow CPU speed still allows the watchdog to be kicked.

7 POWER MANAGEMENT

The TB486 includes sophisticated power management hardware and software, which allows the power consumption of the TB486 to be reduced at times when the full performance of the board is not required. This can extend battery life in battery-operated systems and allow for cooler operation, and thus greater product reliability.

The BIOS can manage power autonomously, without intervention from higher levels of software. It is also compliant with the Advanced Power Management (APM) specification, version 1.2, which can allow APM-aware applications and operating systems to influence the power management of the TB486.

The BIOS default is for the power management to be disabled. Users who do not need power management can ignore this section. Users who do need to save power or to reduce heat should understand this section, and make appropriate settings in the BIOS Setup program.

7.1 OVERVIEW OF POWER MANAGEMENT

The power management on the TB486 relies on a combination of hardware within the Elan processor chip, hardware control of the peripheral functions on the TB486, and power management software.

The way the power management normally operates is as follows.

The user chooses a normal processor clock speed, and determines which peripheral functions are switched on in normal operation. From that point on, hardware within the Elan checks to see whether the computer is doing useful work (as determined by monitoring interrupts, accesses to peripheral functions and so on.) Activities which indicate that the processor is busy constantly reset hardware timers within the Elan, and the TB486 processor is kept at the selected speed, and the selected peripherals remain powered on.

However, during periods of inactivity (while the computer is waiting for user input for example) the activity timers count down and eventually will time out. At this point the TB486 will be switched into a lower power mode. (The timers force a System Management Interrupt, or SMI, and the SMI code is responsible for switching to a lower power mode). As longer periods of inactivity occur the TB486 is switched into lower and lower power modes. At certain points various peripherals can be switched off, and eventually the processor itself is switched off.

The ultimate stage is reached when the processor and most of the peripherals are switched off. At this point the TB486 may draw as little as l0mA from the +5V power supply.

At any point there are a variety of events which will cause the TB486 to switch back to a higher level of operation. To the user the switch is usually imperceptible.

7.2 ELAN POWER MANAGEMENT FEATURES

The Elan processor has been designed with a wealth of power saving features. The features are to a large extent programmable - they can be invoked in one of a number of ways under software control. Some of these features are described here.

The Elan can be thought of as a 486 processor, or CPU, surrounded by peripherals (serial port, interrupt controllers etc). The CPU can be set to execute instructions at a variety of clock speeds. The higher the clock speed the higher the power consumption, and vice versa. The clock can be stopped entirely, so that no instructions are executed. At this point the CPU draws.almost no current. Other elements of the Elan can still be operational at this stage - in particular the power management circuitry stays operating, waiting to bring the CPU back to life by starting its clock.

The CPU runs at several clock speeds. In “High-Speed” mode the CPU can run at 33MHz, 16MHz or 8MHz - these frequencies being software selectable. In “Hyper-Speed” mode the 33MHz clock is doubled (or tripled) to 66MHz (or 100MHz) by a phase locked loop (PLL) clock multiplier. This mode gives the highest performance but also the highest power consumption. (Note that the standard TB486 is not designed to run at 100MHz ‘and reliable operation at this frequency cannot’be guaranteed. If you require 100MHz operation then 100MHz boards can be produced by special order).

Then there is “Low-Speed” mode - programmable as 8Mhz, 4MHz, 2MHz or lMHz. This mode is suitable when not much processing is required, but the CPU must not be shut down entirely.

Then there is “Standby” mode and “Suspend” mode. In these modes the CPU clock is stopped entirely. The main difference between the two modes is that normally the Elan’s phase locked loop clock synthesisers are switched off in Suspend mode for lowest power consumption. When leaving Suspend mode the PLLs must be restarted, which takes a little time. Thus it takes longer to leave Suspend mode for normal operation than it does to leave Standby mode.

Lastly there is “Temporary Low-Speed” mode. On occurrence of certain events the CPU can be taken from Standby mode to Temporary Low-Speed mode in order to execute a relatively small number of instructions, at a low clock rate, before dropping back to Standby mode. In the case of the TB486, Temporary Low-Speed mode is used to service the timer interrupt when it occurs, thus allowing the TB486 to keep track of the DOS time and date, and other routines which may be linked to the timer.

Other Elan features support power management. There are several timers, with programmable time-out periods. If enabled, the expiry of a certain timer will cause the Elan to switch to a lower power mode, or will cause a System Management Interrupt (SMI, see below). The timers are reset to their maximum count if various events are detected by the Elan. These events, which are programmable, include interrupts and software accesses to selected memory or I/O addresses. While these events are occurring the timer cannot time out, and the CPU stays at its current clock speed.

Finally, the internal peripheral functions of the Elan can be shut down when not required, to save power.

The System Management Interrupt, or SMI, is a very high priority interrupt. It is available to allow power management hardware to interrupt the processor in order to request changes to the power management regime. In the case of the TB486, an SMI is generated when the activity timers time out. It is the SMI handling code which forces a switch to a different power state.

While in Standby or Suspend state the DRAM is refreshed by timing circuitry driven by the 32kHz clock. This allows other clocks internal to the Elan to be turned off. The 32kHz clock also provides timing for the power management timers and state machine.

7.3 PERIPHERAL POWER MANAGEMENT FEATURES

Most of the peripherals on the TB486 can be placed into a low power mode by a combination of hardware and software. The Setup program in the BIOS allows many peripherals to be switched off permanently, or selectively as the TB486 enters either Standby or Suspend modes.

The COM1 UART is contained within the Elan chip itself, and can be disabled by software. Other sections of the Elan circuitry will be placed into low power modes as the Elan enters standby or suspend modes.

The 87306 Super I/O chip contains a number of peripherals which can be shut down by software. These include the two serial ports (COM2 and COM3), the printer port, the floppy disk and IDE disk controllers and the keyboard controller.

Key to much of the power saving in the peripheral devices is the Utility Register in the 87306 Super I/O chip. Many of the 16 bits in these two ports are used to shut down peripheral hardware. These are described below, and also in section 3.14.

A signal called ETHEROFF is used to place the CS8900 Ethernet chip into a low power mode.

Two signals - VGAOFF and 32KEN - are used to place the 65550 graphics chip into a low power state, and to route the 32kHz clock to the chip where it is used to keep the video memory refreshed. When in low power mode the 65550 turns off its graphics outputs, and also switches off two signals present on connector J 1 0 - ENAVDD and ENABKL - which can be used to power off a flat panel display and a backlight inverter respectively.

Two signals can be used to shut down the RS-232 and RS-485 transceivers on the serial ports. One signal controls COM1 and the other controls COM2 and COM3. In addition, the UARTS themselves can be placed in low power modes by software.

A signal ADCOFF shuts down the analog to digital converter.

A signal CLOCKOFF turns off the clock synthesiser which produces many clocks for devices outside the Elan chip itself. These include the 14MHz and 8MHz clocks which go to the PC/104 bus, the 14MHz, 20MHz and 24MHz clocks which go to the graphic chip, Ethernet chip and Super I/O chip respectively, and the 1.19MHz clock which drives the Elan's counter/timer unit.

These clocks must not be turned off while there is a requirement for them by their respective peripherals. For example, turning off the clocks will disable the graphics, UARTS, Ethernet chip and any PC/104 bus boards which require the BUSCLK or OSC signals.

7.4 DETAILED OPERATION

The Setup program includes two main menus which influence power consumption.

The first, the Advanced/Integrated Peripherals menu, allows unused peripherals to be turned off permanently. With the peripheral switched off in this menu the BIOS places the device in the lowest possible power state. Its I/O addresses and interrupt become available for other devices on the PC/104 bus. Once off the peripheral remains off, and is not dynamically controlled by the power management process.

The second, the Power menu, defines the dynamic power saving operation.

In the Power menu, the Power Savings item allows dynamic power management to be switched off, or placed in one of two pre-configured modes (termed Maximum Performance and Maximum Power Savings), or customised. The pre-configured and customised modes enable a number of timers. In the customised mode the periods of these timers can be adjusted.

These timers define the amount of time which elapses before the TB486 is switched into the next lowest power mode, in the absence of “events” which act to reset the timers. For example, in the “Maximum Power Saving” setting, assuming that the computer is running DOS and waiting for user input from the keyboard, the following will occur.

One second after the last keyboard activity the TB486 will switch from Hyper-Speed mode to High-Speed (assuming that it has been operating at Hyper-speed - 66MHz or 100MHz). One second later it will switch from High-Speed mode to Low-Speed mode. One minute later it will switch into Standby mode (the CPU clock is stopped except to service the timer interrupt). Finally, two minutes later, the TB486 will switch into Suspend mode (not even the timer interrupt is serviced).

Note that the TB486 will only be in the Hyper-Speed mode if the CPU Clock has been set to 66MHz or 100MHz in the Advanced/Advanced Chipset Control menu. Otherwise the highest speed mode will be the High-Speed mode.

If one of the timers is set to “off’ then the timer will never time out, and the next lowest state will not be entered. For example, if the Low Speed timer is set to “off’ the TB486 will power down to the High-Speed mode, but will not enter the Low-Speed mode, nor will it enter the lower power modes: Standby mode and Suspend mode.

Table 6 lists the power modes and describes the activities in each state.

Mode	CPU Clock	CPU Activity	Peripheral Activity
Hyper-Speed	66, 100MHz	CPU fully operational at highest speed.	Peripherals are on.
High-Speed	33, 16 or 8MHz	CPU fully operational at relatively high speed.	
Low-Speed	8, 4, 2 or 1MHz	CPU fully operational but processor speed is low.	
Standby	Stopped	CPU clock stopped, except to service timer interrupts. Elan enters Temporary Low Speed mode to service the timer.	Mant peripherals can be shut down. These are selected by the Setup program.
Suspend	Stopped	CPU clock stopped, PLL synthesisers stopped. Timer interrupt not serviced.	
Temporary Low-Speed	Same as Low-Speed	Elan enters this state on a timer interrupt. It remains in this state for a fixed time before returning to Standby.	Same as for Standby mode.

TABLE 6 - POWER MODES

The menu called Device Power Down allows the user to determine which peripherals are switched off when the TB486 enters Standby mode, and which are switched off when the TB486 enters Suspend mode.

Certain “events” can cause the TB486 to switch from one mode to another. Events are such things as interrupts, software accesses to peripheral I/O locations, DMA requests, and inputs on some I/O signals.

Some events cause the TB486 to remain in Hyper-Speed mode or High-Speed mode. Other events can cause the TB486 to return to Hyper-Speed mode or High-Speed mode from the Low-Speed mode. Still other events can cause the TB486 to return to Hyper-Speed mode or High-Speed mode from the Standby or Suspend states. Some of these events ‘are permanently selected by the BIOS, and will always cause a change of mode. Other events can be selected by the Wakeup Events menus to cause a change of mode. Table 7 lists events which can cause state transitions in each mode.

For example, the first entry in Table 7 shows that keyboard and mouse activity will always keep the TB486 in Hyper-Speed mode. Additional activities (hard and floppy disk activity, sedal and parallel port activity) can be programmed to keep the Tb486 in the Hyper-Speed mode. The additional modes are enabled using the Setup program’s Power/Wakeup Events High/Low Speed menu.

To use COM2 or COM3 to force a resume from standby (?) or suspend the serial port must be programmed to generate an interrupt. It is the arrival of the interrupt which forces the resume. The programmable interrupt controller (PIC) must also be programmed to accept the interrupt, and the interrupt must be unmasked.

In Suspend mode (only?) it is possible to use an RTC alarm interrupt to force a resume. This allows the user to set the alarm for some time in the next 24 hours, force a suspend, and then expect to resume again at the pre-arranged time. The programmable interrupt controller (PIC) must also be programmed to accept the interrupt, and the interrupt must be unmasked. Sample code on the TB486 Utilities Disk gives an example of how to do this.

Current Mode	Next Mode	Events Causing Change (always)	Events Causing Change (optional)
Hyper-Speed	Hyper-Speed	Keyboard or Mouse activity will keep Elan in this mose	Events enabled in Wakeup Events High/Low Speed menu, disk drives, Com1, Com2 and printer activity
	High-Speed	None	High Speed Timer times out
	Standby	APM Standby Request	None
	Suspend	APM Suspend Request	None
High-Speed	Hyper-Speed if enabled, else High-Speed	Keyboard or Mouse activity	Events enabled in Wakeup Events High/Low Speed menu, disk drives, Com1, Com2 and printer activity
	Low-Speed	None	Low Speed Timer times out
	Standby	APM Standby Request	None
	Suspend	APM Suspend Request	None
Low-Speed	Hyper-Speed if enabled, else High-Speed	Keyboard or Mouse activity	Events enabled in Wakeup Events High/Low Speed menu, disk drives, Com1, Com2 and printer activity
	Standby	APM Standby Request	Standby Timer times out
	Suspend	APM Suspend Request	None
Standby	Hyper-Speed if enabled, else High-Speed	Keyboard or Mouse activity	Events enabled in Wakeup Events Standby/Suspend Speed menu Com1, Com2 activity
	Suspend	None	Suspend Timer times out
	Temporary Low-Speed	Timer Interrupt (IRQ0)	None
Suspend	Hyper-Speed if enabled, else High-Speed	Keyboard or Mouse activity	Events enabled in Wakeup Events Standby/Suspend Speed menu Com1, Com2 , Com3, RTC activity
Temporary Low-Speed	Standby	Timer times out	None

TABLE 7 - EVENTS WHICH CAUSE A MODE CHANGE

7.5 APM SOFTWARE INTERFACE

The TB486 power management can be controlled by application software. This is done by use of the Advanced Power Management (APM) interface. APM code is included in

the BIOS. Application programs can communicate with the APM code by making BIOS calls. This allows the application to move the TB486 from one power mode to another.

Details on how to use APM are to follow later.

Sample code is included on the TB486 Utilities Disk showing how to force the TB486 into Standby or Suspend from within an application program.

7.6 POWER CONSUMPTION MEASUREMENTS

The power consumption of the TB486 depends mainly on the speed of the processor clock, and which peripherals are powered on. The processor clock speed can be fixed using the Setup program, and the power management software can vary the processor clock dynamically. The peripherals can be powered on or off permanently using the Setup program, or dynamically under the control of the power management software.

There are other factors which also affect the power consumption. The program being executed will affect power consumption - some instruction sequences cause the processor and memory to draw more current than other sequences. The DRAM fifted also has an effect - as a general rule, the more DRAM chips that are used on a DIMM module the higher the power consumption. And of course peripheral devices and other PC/104 boards will also draw current, and will influence the current taken by the TB486 itself.

The figures given in this section are therefore only “typical” figures - measurements in real-world applications are likely to vary somewhat.

The measurements given here were made with a TB486 running in stand-alone mode (not plugged into a PC/104 bus or development system). Unless otherwise noted the configuration was as follows. The DRAM used was a 16Mbyte module using eight 4M x 4 DRAM chips. The connected peripherals were a 3½" floppy disk drive, an AT keyboard and a CRT monitor (the figures do not include the power drawn by these peripherals). The TB486 was allowed to boot MS-DOS from the floppy, and measurements were taken with the computer sifting at the A: prompt waiting for keyboard input.

The power management software was then allowed to switch the TB486 into progressively lower power states, and power measurements were taken.

In addition, peripherals were switched off, either permanently or dynamically, and this allowed us to determine approximately the power consumption of each of the peripheral devices. Note that, with the exceptions noted above, no peripherals were connected. It is possible that power consumption could vary if real peripherals were connected to the TB486 (for example, an RS-232 transceiver is likely to draw more current if it is connected to a printer than it is unused).

Table 8 gives the power consumption for the TB486 as a whole in a number of power states, with all peripherals switched on. Two measurements were made, one at the DOS prompt, with the processor waiting for keyboard input, and the other running the extended memory test from the Checkit test program.

Table 9 provides the same data as Table 8, but with the graphics and Ethernet chips switched off. These two peripherals draw considerable current; Table 9 will provide typical figures for the TB486 in applications which are not using graphics or Ethernet.

Mode	Power Consumption (mA)	
	DOS Prompt	Checkit
Hyper-Speed, 100MHz	786	860
Hyper-Speed, 66MHz	650	735
High-Speed, 33MHz	502	579
High-Speed, 16MHz	414	547
High-Speed, 8MHz	374	427
Low-Speed, 8MHz	374	N/A
Low-Speed, 4MHz	354	
Low-Speed, 2MHz	343	
Low-Speed, 1MHz	338	
Standby (and Temp Low-Speed for timer IRQ)	334	
Suspend	328	

TABLE 8 - TB486 POWER, ALL PERIPHERALS ON

Mode	Power Consumption (mA)	
	DOS Prompt	Checkit
Hyper-Speed, 100MHz	491	537
Hyper-Speed, 66MHz	358	416
High-Speed, 33MHz	208	251
High-Speed, 16MHz	124	157
High-Speed, 8MHz	85	112
Low-Speed, 8MHz	85	N/A
Low-Speed, 4MHz	65	
Low-Speed, 2MHz	58	
Low-Speed, 1MHz	53	
Standby (and Temp Low-Speed for timer IRQ)	51	
Suspend	46	
Suspend with all peripherals off and clock generator off	10	

TABLE 9 - TB486 POWER, GRAPHICS AND ETHERNET OFF

Table 10 shows how the power consumed by the Elan and memory varies with different DRAM memory modules. The measurements were taken in 66MHz Hyper-Speed mode with all peripherals on. The Table 10 data can be used to modify the Table 8 and Table 9 figures to give more accurate estimates of power consumption with a variety of memory configurations.

The current taken at the DOS prompt is almost completely unaffected by the DRAM used, presumably because the processor is executing almost exclusively from its cache. Note also that the currents taken by the DIMM modules is likely to vary with manufacturer and DRAM technology used.

DRAM Memory Fitted	Power Consumption (mA)	
	DOS Prompt	Checkit
64MBytes (8 chips)	653	769
32MBytes (4 chips)	650	775
16MBytes (8 chips)	651	735
8MBytes (4 chips)	651	712
4MBytes (2 chips)	657	715

TABLE 10 - TB486 POWER, DIFFERENT DRAM MODULES

Table 11 provides estimates of the power consumption of each of the main elements of the TB486 - processor, peripherals and memory. This provides a break-down of the current drawn when the processor is running in 66MHz Hyper-Speed mode with all the peripherals on. The Table 1 1 data can be used to modify the Table 8 and Table 9 figures to give more accurate estimates of power consumption with a particular mix of peripherals enabled.

Element	Power Consumption (mA)
Elan and memory running at 66MHz	316
Graphics	188
Ethernet	103
Floppy Disk	0
IDE Disk	0
Serial Ports	4
Printer Port	0
Clock Generator	29
Keyboard Controller	0
Residual 87306 Current	7
Residual Elan and miscellaneous current	3
Total	650

TABLE 11 - POWER CONSUMPTION OF TB486 ELEMENTS

APPENDIX A: SPECIFICATION

Product:	TB486
Description:	Highly-integrated PC/104 format, single board PC compatible computer.
Processor:	AMD Elan SC410. Clock speed of 100MHz maximum, with many lower clock speeds available for power savings. (66MHz processor fifted as standard).
DRAM:	4M, 8M, 16M, 32M or 64M bytes DRAM implemented using 72-pin DIMM memory modules (EDO, 3.3V).
Flash Memory:	2M byte of AMD 29F016 Flash memory. (The default is for 2M bytes of Flash memory; the TB486 can be fifted with 4M bytes as a special order).
Graphics Controller:	Chips and Technologies 65550 with 2M bytes video DRAM. Can drive CRT and flat panel displays up to 1600 x 1280.
Floppy Disk Controller:	Drives single 3½ inch floppy disk drive through 26-way flat flexible cable.
IDE Disk Controller:	Drives two [DE devices - hard disk drives or CD-ROMS.
Ethernet Controller:	Crystal Semiconductor CS8900. 10Base-T with external RJ-45 module.
Printer port:	Centronics compatible (PRN). Bi-directional. EPP and ECP compatible.
Serial interface:	RS-232 (COM1, COM2 and COM3). RS-485 full-duplex or half-duplex option for COM2.
Keyboard port:	IBM AT compatible.
Mouse port:	PS/2 compatible.
Speaker port:	IBM AT compatible.
A/DConverter:	Four channel, 12-bits. External reference. 0V to +5V input range.
Reset circuit:	Power supply monitor, PC/104 bus reset, watchdog timer and external reset switch capability.
Bus interface:	PC/104 V2.3 16-bit
Interrupts:	Standard PC and PC/AT interrupts are available for on-board peripherals or the PC/104 bus: (IRQ3, IRQ5, IRQ6, IRQ7 or IRQ8, IRQ10, IRQ12, IRQ14).
DMA:	Standard PC and PC/AT DMA request and acknowledge pairs available on PC/104 bus. (DREQ2/DACK2 and DREQ1/DACK1 or DREQ7/DACK7) Multiple bus masters (using the /MASTER signal) are not supported.
Connectors:	Standard PC/104 8-bit and 16-bit stack-through connectors. Non-stack-through connectors optionally available. A 10-way, 16-way and 50-way right-angle headers for I/O. A 4-way right angle Molex power connector. A 26-way flat flexible cable for a floppy drive. A 44-way 2mm straight connector for IDE drives. A 40-way 0.05" connector for flat panels. An 8-pin SIL header for Ethernet.
Dimensions:	PCB - 3.550 inches * 3.775 inches, (91.7 mm * 95.8 mm Approx.) overall dimensions including connectors, 4.25 inches * 4 inches, (108mm * 102mm approx.). Maximum height on the component side of the PCB is 11.0mm.

Weight:	95g Approx.
Operating temperature:	0 - 60 ºC.
Humidity:	10% - 90% non-condensing.
Power Supplies:	+5V only required. 786mA typ (100MHz, all peripherals on) 650mA typ. (66MHz, all peripherals on) 208mA typ. (33MHz, Ethernet and graphics off) 228mA typ (standby, Ethernet and graphics oft) l0mA typ (suspended, all peripherals off) See section 7.6 for power consumption of other configurations.

APPENDIX B: TB486 SET-UP PROCEDURE.

The component placement diagrams in Appendix C may be of help in locating components referred to in this appendix.

B.1 DRAM CONFIGURATION

The standard TB486 product is delivered with no DRAM DIMM modules fifted as standard. Users may buy DIMM modules from DSP Design or fit their own. DSP Design carry stock of the DIMM modules. These modules have been selected to operate correctly with the TB486.

DRAM should be 70ns or faster, and must be designed for 3.3V operation, not 5V. Table B1 lists the DSP Design part numbers for various memory sizes.

DRAM SIZE DSP DESIGN PART

DRAM Size	DSP Design Part No
4 MBytes	LD4
8 MBytes	LD8
16 MBytes	LD16
32 MBytes	LD32
64 MBytes	LD64

TABLE B1 - DIMM MODULES

Install your DRAM DIMM module in the TB486 DRAM socket, observing its polarity, and observing proper anti-static precautions. The DIMM socket has a lug which engages with a cut-out on the module, which prevents incorrect installation.

B.2 SOLDER LINK AREAS

A number of functions can be configured with solder links on the TB486 board. The board layout is so dense we have implemented these configuration options with solder links which take less space than jumpers, as well as being more reliable.

Care must be taken when changing these link areas so that no accidental shorts are produced or created. Default settings are noted below.

(Note that these are the settings for the REV C board. REV B boards have some differences.)

LK1 POWER SUPPLY VOLTAGE

This link affects the output voltage of the on-board switch mode power supply. It is factory set and must not be altered.

LK2 A/D CONVERTOR REFERENCE

This link is used to select the source of the VREF- input voltage to the analog to digital converter. Note that when the link is fitted the on-board +5V power supply is not only connected to the A/D converter VREF pin, but is also taken out to the VREF pin on connector J9.

VREF is supplied by on-board +5V:	Fit Link (default).
VREF is supplied from an external source:	Omit Link.

LK3 A/D CONVERTOR INPUT ADC3

This link is used to connect the analog to digital converter input ADC3 to the on-board temperature sensor.

ADC3 is connected to on-board temperature sensor: Install link (Default setting)
ADC3 may be supplied externally: Omit link.

LK4 REMOTE BOOTSTRAP

This link needs to be set according to the location of the BIOS. It is normally only used in the manufacturing process.

BIOS is in the Flash memory:	Install link. (Default setting)
BIOS is in off-board EPROM:	Do not install link.

LK5 COM2 RS-232/RS-485 SELECTION

This link is used to select whether COM2 is RS-232 or RS-485.

RS-232:	Link installed. (Default setting)
RS-485	No link installed.

LK6 PIRQ5 LINK

This link is used to select the source of the Elan's PIRQ5 interrupt pin.

PIRQ5 is driven by IRQ7 from printer:	Link 1 - 2.
PIRQ5 is driven by IRQ8 from RTC:	Link 2 - 3. (Default setting)

APPENDIX C: COMPONENT PLACEMENT DIAGRAMS

The two component placement diagrams which follow (one for each side of the TB486) may be of help in locating the components referred to in Appendix B.

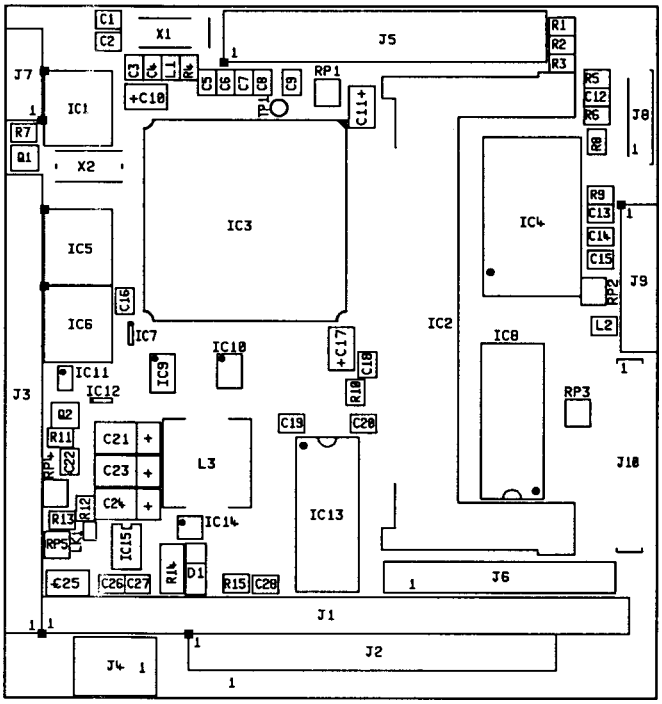

FIGURE CI - TOP COMPONENT PLACEMENT DIAGRAM

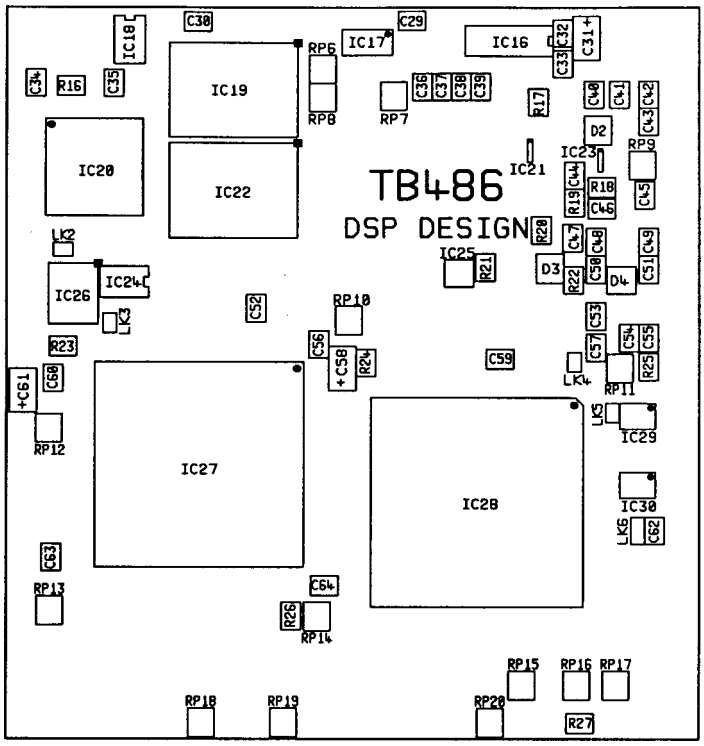

FIGURE C2 - BOTTOM COMPONENT PLACEMENT DIAGRAM

APPENDIX D: OPTIONS AND ORDERING INFORMATION

This Appendix lists some of the range of PC/104 products available from DSP Design, and in particular the products related to the TB486. Note that as new products are being released all the time this list may not be complete. Contact your supplier for a full price list.

Note that the standard TB486 is fifted with no DRAM.

PROCESSOR BOARD

TB486 Standard TB486 processor board, without DRAM.

DRAM

LD4	4M byte DIMM DRAM module
LD8	8M byte DIMM DRAM module
LD16	16M byte DIMM DRAM module
LD32	32M byte DIMM DRAM module
LD64	64M byte DIMM DRAM module

ACCESSORIES

The following part numbers should be used to order various accessories:

TBPAK486	Starter pack including TB486, TCDEV, TB486-UTILS, TRM-TB486 and TCPSU. DRAM is ordered separately.
TB486-UTILS	Utilities disk for TB486
TRM-TB486	Technical reference manual. CF100 Solid-state IDE disk drive.
TB486ET	Ethernet adapter board for TB486
TB486ET-CAB	Cable assembly to connect TB486 and TB486ET
TFT6-KIT 6.4"	TFT LCD kit, including 6.4" high-brightness LCD display, backlight inverter, TFTIF31 interface board, TFTIF-CAB1 1 40-way ribbon cable and cable for backlight inverter.
TFTIF31	Display adapter board - plugs into Sharp 640 x 480 TFT displays and accepts input from TB486.
TFTIF41	Display adapter board - plugs into Sharp 800 x 600 TFT displays and accepts input from TB486.
TFTIF15	Display adapter board - plugs into Hosiden 1024 x 768 TFT displays and accepts input from TB486.
TFTIF-CAB11	40-way cable assembly for flat panel displays, connector at both ends, length 11 inches.
EC586-LCA	40-way cable assembly for flat panel displays, connector at one end, length 10 inches.
TB486-COM3CA	Cable assembly - connects TB486 J7 to a 9-way D-type connector.
TB486-CRTCA	Cable assembly - connects TB486 J9 to a 15-way VGA CRT connector.
TCDEV	PC/104 Development Platform.
TCPSU	Power supply unit for the TCDEV.
TCDOS	Microsoft MS-DOS Operating System.
TCWIN	Windows 3.1 operating system.
WIN95FL	Windows 95 operating system.
TCSPACER	PC/104 spacer kit - four 0.6 inch spacers plus nuts and screws.
COMM-DRVDOS	DOS Serial Communications Driver Software
IDE-3020	Cable to convert 2½ inch IDE connector to 3½ inch IDE connector and vice-versa

DIS26	3.5 inch floppy disk.drive with 26-way connector
DIS26-CAB	26-way flat flexible cable for DIS26 floppy disk drive.
EC586-IDECA	Cable to connect the TB486 to 2½ inch IDE drives
TCDISK-2100	2.1 G byte 2½ inch IDE drive

PC/104 MODULES

The following list describes a selection of the PC/104 bus cards that are available from DSP Design. Contact your supplier for the latest list.

I/O MODULES

TCMCIB-2	Two slot PCMCIA interface board.
TP024	Opto-isolated I/O board. Twelve inputs and twelve outputs
TP406	Parallel I/O and timer board. Forty lines of parallel I/O
TS400	Four serial interfaces on one board
TAD-12	12-bit Analogue to Digital converter board
TCAUDIX	Audio board (Soundblaster-compatible)
TCMPEG	MPEG-1 playback board

FLASH DISKS

The two Tiny Flash Disk modules listed below are PC/104 modules which can be added to the TB486 to provide Flash File System memory in excess of that provided by the on-board Flash chip. They have PC/104 connectors, but are much smaller than PC/104 size. The eight Flash Disk boards listed below are full PC/104 sized boards. The Tiny Flash Disks cannot be used concurrently with the TB486 Flash File System.

TFD-01	1M byte PC/104 Tiny Flash Disk module
TFD-04	4M byte PC/104 Tiny Flash Disk module

TCFL01M	1M byte PC/104 Flash Disk Board
TCFL02M	2M byte PC/104 Flash Disk Board
TCFL04M	4M byte PC/104 Flash Disk Board
TCFL08M	8M byte PC/104 Flash Disk Board
TCFLO10M	10M byte PC/104 Flash Disk Board
TCFLO16M	16M byte PC/104 Flash Disk Board
TCFLO20M	20M byte PC/104 Flash Disk Board
TCFLO32M	32M byte PC/104 Flash Disk Board

APPENDIX E: CONNECTOR PIN ASSIGNMENTS

E.1 BUS CONNECTORS

The PC/104 bus connectors Jl and J2 have pin assignments which conform to the PC/1,04 bus specification V2.3. The pin assignments are shown below.

Pin	J1	
	Row A	Row B
1	/IOCHCHK	0V
2	SD7	RESETDRV
3	SD6	+5V
4	SD5	IRQ9
5	SD4	-5V *
6	SD3	DRQ2 **
7	SD2	-12V *
8	SD1	/ENDXFR
9	SD0	+12V *
10	IOCHRDY	(KEY)
11	AEN	/SMEMW
12	SA19	/SMEMR
13	SA18	/IOW
14	SA17	/IOR
15	SA16	/DACK3 ***
16	SA15	/DRQ3
17	SA14	/DACK1 **
18	SA13	DRQ1 **
19	SA12	/REFRESH ***
20	SA11	SYSCLK
21	SA10	IRQ7
22	SA9	IRQ6
23	SA8	IRQ5
24	SA7	IRQ4 *
25	SA6	IRQ3
26	SA5	/DACK2 **
27	SA4	TC
29	SA3	BALE
29	SA2	+5V
30	SA1	OSC
31	SA0	0V
32	0V	OV

Pin	J2	
	Row C	Row B
0	0V	0V
1	/SBHE	/MEMCS16
2	LA23	/IOCS16
3	LA22	IRQ10
4	LA21	IRQ11
5	LA20	IRQ12
6	LA19	IRQ15
7	LA18	IRQ14
8	LA17	/DACK0
9	/MEMR	DREQ0
10	/MEMW	/DACK5
11	SD8	DRQ5
12	SD9	/DACK6
13	SD10	DRQ6
14	SD11	/DACK7
15	SD12	DRQ7
16	SD13	+5V
17	SD14	/MASTER*
18	SD15	0V
19	(KEY)	0V

* These connections are not implemented on the TB486
** See Section 4.6 for a discussion on DMA
*** These pins are pulled to logic 1

TABLE El - PC/104 J1 PIN ASSIGNMENTS
TABLE E2 - PC/104 J2 PIN ASSIGNMENTS

Pins 0 and 19 of J2 connector are marked on the PCB silk-screen with a “O” and “19” respectively, and rows C and D are also marked.

Pins 1 and 32 of J1 connector are marked on the PCB silk-screen with a “1” and “32” respectively, and rows A and B are also marked.

E.2 TB486 PERIPHERAL CONNECTOR

Most peripheral devices are connected to the TB486 through a 50 way IDC connector, called J3. The 50 pins on the connector are brought to the outside world through a 50 way 0.1 inch IDC right angled connector.

The J3 connector pin assignments are almost identical on all DSP Design PC/104 processor boards. The TB486 pin assignments are identical to the TC586 and TX486 pin assignments. However there are two minor differences between the TB486 and the TC386/TC486 boards, which users who are updating from TC386 or TC486 boards should note:

1 Pins 1 and 2 are IRDA pins on the TB486 and power supply pins on the TC386/TC486.

2 When using COM2 in RS485 mode the RS485 A and B pins (pins 37 and 38) are transposed between theTB486 and the TC386fTC486.

Table E4 lists the J3 signal name and also the peripheral to which the signal belongs and the pin number of that peripheral's connector. The standard connectors used in PC's for each of the peripherals are:

Centronics Printer:	25 way female D-type
Keyboard:	5 way female circular DIN
Mouse:	6 pin mini DIN (PS/2 style)
Serial COM1:	9 way male D-type Serial
COM2:	9 way male D-type
Loudspeaker:	N/A
Baftery:	N/A
Reset Switch:	N/A

Pin 1 of the J3 connector can be identified by looking at the J3 silk-screen box which surrounds the J3 connector on the TB486. A "2" is located close to the pin 1 end of J3 and a "49" is placed close to the pin 50 end. All odd numbered pins are in one row and all even numbered pins are in the other row.

Table E3 shows how J3 pins change function when COM2 is used for RS-485 operation.

RS-485	RS-232	J3 Pin
Transmit, inverting	DTR1	35
Transmit, non-inverting	CTS1	36
Receive, inverting	TXD1	37
Receive, non-inverting	RTS1	38

TABLE E3 - RS485 FUNCTION OF COM2 SERIAL PORT

NOTES: * J3 pin 13 connects to printer port D-type connector pins 18 to 25 inclusive. ** Pins 35 - 38 carry RS485 signals when COM2 operates as an RS-485 port. See Table E3 for details.

Pin	Peripheral	Signal	J3	J3	Signal	Peripheral	Pin
	IRDA	IRRX	1	2	IRTX	IRDA	
5	Mouse	MCLOCK	3	4	MDATA	Mouse	1
13	Centronics	SLCT	5	6	PE	Centronics	12
11		BUSY	7	8	/ACK		10
9		PD7	9	10	PD6		8
7		PD5	11	12	PD4		6
*		GND	13	14	PD3		5
17		/SLCTIN	15	16	PD2		4
16		/INIT	17	18	PD1		3
15		/ERROR	19	20	PD0		2
14		/AUTOFD	21	22	/STROBE		1
	Reset	GND	23	24	/RESET	Reset	
	Speaker	VCC	25	26	SPKR	Speaker	
	Battery	GND	27	28	BATT	Battery	
5	Keyboard	VCC	29	30	KBDATA	Keyboard	2
4		GND	31	32	KBCLK		1
5	Com2	GND	33	34	RI1	Com2	9
4		DTR1	35	36	CTS1		8
3		TXD1	37	38	RTS1		7
2		RXD1	39	40	DSR1		6
1		DCD1	41	42	GND	Com1	5
9	Com1	RI0	43	44	DTR0		4
8		CTS0	45	46	TXD0		3
7		RTS0	47	48	RXD0		2
6		DSR0	49	50	DCD0		1

*: J3 pin 13 connects to Centronics Port pins 18 to 25 inclusive.
Pins 35 - 38 carry RS-485signals when Com2 operates as an RS-485 port. See Table E3

TABLE E4 - J3 I/O CONNECTOR PIN ASSIGNMENTS

E.3 J4 POWER CONNECTOR

The J4 connector is used to provide an alternate power inlet to the TB486 for stand-alone operation. The J4 connector uses industry standard parts and a number of manufacturers are able to provide suitable mating connectors.

The J4 connector used on the TB486 is a Molex mini KK, 2.5mm pitch, 5046 series right-angled header with friction lock. A suitable mating half would be the MOLEX mini KK 2.5mm pitch 5051 series crimp polarizing housing. Crimp pins are required for this housing connector and these are also available from Molex. At the time of writing, Farnell Electronic Services supply these Molex parts as standard with the stock numbers 011007D for the polarized housing connector and 011122R for the crimp pins.

J4 Pin	Signal
1	GND
2	GND
3	VCC
4	VCC

TABLE E5 - J4 POWER CONNECTOR PIN ASSIGNMENTS

Pin 1 of the J4 connector can be identified by looking at the silk-screen legend on the TB486 PCB. Pin 1 has a ‘l’to the right hand side of the Gonnector.

E.4 J5 IDE CONNECTOR

The IDE drive is connected through J5, a straight 2mm pitch 44-way connector. Pin assignments follow.

Signal	J5 Pin	J5 Pin	Signal
/RESET	1	2	GND
ID7	3	4	ID8
ID6	5	6	ID9
ID5	7	8	ID10
ID4	9	10	ID11
ID3	11	12	ID12
ID2	13	14	ID13
ID1	15	16	ID14
ID0	17	18	ID15
GND	19	20	N/C
N/C	21	22	GND
/IOW	23	24	GND
/IOR	25	26	GND
IOCHRDY	27	28	ALE
N/C	29	30	GND
IRQ14	31	32	/IOCS16
A1	33	34	GND
A0	35	36	A2
/CS0	37	38	/CS1
N/C	39	40	GND
VCC	41	42	VCC
GND	43	44	VCC

TABLE E6 - J5 IDE CONNECTOR PIN ASSIGNMENTS

Pin 1 of J5 can be identified by a “1” close to pin 1 of the connector. E.5 J6 FLOPPY CONNECTOR

E5 J6 FLOPPY CONNECTOR

Signal	J6 Pin	J6 Pin	Signal
Vcc	1	2	/INDEX
	3	4	/DS0
	5	6	/DSKCHG
N/C	7	8	N/C
	9	10	/M0
	11	12	/DIRC
	13	14	/STEP
GND	15	16	/WD
	17	18	/WE
	19	20	/TK00
	21	22	/WPT
	23	24	/RDATA
	25	26	/HS

TABLE E7 - J6 FLOPPY CONNECTOR PIN ASSIGNMENTS

Pin 26 of the J6 connector can be identified by a small “26” on the top of the plastic molding of the connector.

E.6 J7 COM3 SERIAL PORT CONNECTOR

Connector J7 is a 10-way pin header adjacent to J3. It carries the COM3 serial port signals. The signals are arranged so that a ribbon cable from J7 can easily crimp onto a 9-pin IDC D-type connector..

Signal	J7 Pin	J7 Pin	Signal
GND	1	2	RI2
DTR2	3	4	CTS2
TXD2	5	6	RTS2
RXD2	7	8	DSR2
DCD2	9	10	VCC

TABLE E8 - J7 COM3 CONNECTOR PIN ASSIGNMENTS

Pin 1 of the J7 connector can be identified by looking at the silk-screen legend on the TB486 PCB. “9” and “10” appear close to pins 9 and 10.

E.7 J8 ETHERNET CONNECTOR

Connector J8 is an 8-way SIL header. It carries'the Ethernet controller signals to a remote PCB, the TB486ET, which carries the Ethernet isolation transformer and RJ45 connector. The connector is from the Hirose DF13 family.

J8 Pin	Signal
1	RxD+
2	RxD-
3	Vcc
4	GND
5	/LINKED
6	/LANLED
7	TxD-
8	TxD+

TABLE E9 - J8 ETHERNET CONNECTOR PIN ASSIGNMENTS

Pin 1 of the J8 connector can be identified by looking at the silk-screen legend on the TB486 PCB. A'l'symbol is placed close to pin 1.

E.8 J9 A/D CONVERTOR AND CRT CONNECTOR

Connetor J9 is a 16-pin right angle pin header. It carries the analog to digital converter signals and the signals for a VGA CRT display. Also included on the connector is the Elan suspend/resume signal.

The VGA CRT display signals are usually connected to a 15-pin high density D-type connector. Pin assignments for this connector are also given in the table.

NOTE: Pin 9 is SUS-RES on REV C boards and ADCGND on REV B boards.

VGA Pin	Signal	J9 Pin	J9 Pin	Signal	VGA Pin
	VREF	1	2	ADC0	
	ADCGND	3	4	ADC1	
	ADCGND	5	6	ADC2	
	ADCGND	7	8	ADC3	
	SUS_RES	9	10	RED	1
2	GREEN	11	12	BLUE	3
6, 7, 8	AGND	13	14	HSYNC	13
14	VSYNC	15	16	GND	5, 10

TABLE E10 - J9 VGA AND A/D CONNECTOR PIN ASSIGNMENTS

E.9 J10 FLAT PANEL CONNECTOR

The flat panel display is connected through J10, a straight 0.05" pitch 40-way pin header. Pin assignments are shown in Table E11. The signals change their function depending on the display type being used. Table E12 lists the uses of the signals for a variety of display types. Table E13 describes the functions of the signals. The LCD panel signal names and may vary from panel to panel, however the signal descriptions should remain virtually the same. Use Tables E11, E12 and E13 to help you create an interface cable to connect between the TB486 and your flat panel.

Signal	J10 Pin	J10 Pin	Signal
ENABKL	1	2	ENAVDD
GND	3	4	SHFCLK
GND	5	6	LP
GND	7	8	FLM
P16	9	10	P17
P18	11	12	P19
GND	13	14	P20
P21	15	16	P22
GND	17	18	P23
P8	19	20	P9
GND	21	22	P10
P11	23	24	P12
3.3V	25	26	P13
P14	27	28	P15
3.3V	29	30	P0
P1	31	32	P2
Vcc	33	34	P3
P4	35	36	P5
Vcc	37	38	P6
P7	39	40	M

TABLE E11 - J10 FLAT PANEL CONNECTOR PIN ASSIGNMENTS

	Mono			Colour							
	SS	DD	DD	TFT	TFT	TFT HR	STN SS	STN SS	STN DD	STN DD	STN DD
J10 Pin Name	8-bit	8-bit	16-bit	9/12/16 bit	18/14 bit	18/24 bit	8-bit (X4bp)	16-bit (4bp)	8-bit (4bp)	16-bit (4bp)	24-bit
P0		UD3	UD7	B0	B0	B00	R1	R1	UR1	UR0	UR0
P1		UD2	UD6	B1	B1	B01	B1	G1	UB1	UG0	UG0
P2		UD1	UD5	B2	B2	B02	G2	B1	UG1	UB0	UB0
P3		UD0	UD4	B3	B3	B03	R3	R2	UR2	UR1	LR0
P4		LD3	UD3	B4	B4	B10	B3	G2	LR1	LR0	LG0
P5		LD2	UD2	G0	B5	B11	G4	B2	LG1	LG0	LB0
P6		LD1	UD1	G1	B6	B12	R5	R3	LB1	LB0	UR1
P7		LD0	UD0	G2	B7	B13	B5	G3	LR2	LR1	UG1
P8	P0		LD7	G3	G0	G00	SHFCLKU	B3		UG1	UB1
P9	P1		LD6	G4	G1	G01		R4		UB1	LR1
P10	P2		LD5	G5	G2	G02		G4		UR2	LG1
P11	P3		LD4	R0	G3	G03		B4		UG2	LB1
P12	P4		LD3	R1	G4	G10		R5		LG1	UR2
P13	P5		LD2	R2	G5	G11		G5		LB1	UG2
P14	P6		LD1	R3	G6	G12		B5		LR2	UB2
P15	P7		LD0	R4	G7	G13		R6		LG2	LR2
P16					R0	R00					LG2
P17					R1	R01					LB2
P18					R2	R02					UR3
P19					R3	R04					UG3
P20					R4	R10					UB3
P21					R5	R11					LR2
P22					R6	R12					LG3
P23					R7	R13					LB3
SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK
Pixels/ Clock	8	8	16	1	1	2	2 - 2/3	5 - 1/3	2 - 2/3	5 - 1/3	8

TABLE E12 - FLAT PANEL DATA SIGNALS

Signal Name	Signal Function
P0 - P23	Display Data
SHFCLK	Shift Clock. Pixel clock for flat panel displays
FLM	First Line Marker. Flat panel equivalent of VSYNC
LP	Latch Pulse. Flat panel equivalent of HSYNC
M	M signal for panel AC drive on mono LCDs. Configured as Display Enable or BLANK-TFT panels.
ENAVDD	Power sequencing control for Vdd. High to switch on power
ENABKL	Power sequencing control for Vbacklight inverter. High to switch on power

TABLE E13 - FUNCTION OF FLAT PANEL SIGNALS

APPENDIX F: TFTIF FLAT PANEL INTERFACE BOARDS

F.1 INTRODUCTION

The TFTIFxx boards are a family of small PCBs which mount onto some TFT LCD displays. They accept LCD signals from the TB486 flat panel connector J10 processor board via a length of high-density 40-way ribbon cable. These signals are then re-arranged on the PCB and routed to the correct pins on the LCD.

At present there are four boards in the family, as shown in Table Fl. When this appendix has to refer to all members of the family it uses the term “TFTIFXX”. Slightly confusingly, one board is called TFTIF, without additional numbers to further identify it. The TFTIF31, TFTI F41 and TFTIF15 boards are newer than the TFTIF, and provide some additional features.

Interface Board	Display			Supply Voltage	Connector on Display
	Model	Mfgr	Resolution		
TFTIF	LP121S1	LG Electronics	800 x 600	+3.3Vdc	DF9-41S-1V
TFTIF31	LQ10D42 LQ64D341	Sharp	640 x 480	+5Vdc	DF9-31S-1V
TFTIF41	LQ12S41	Sharp	800 x 600	+3.3Vdc	DF9-41S-1V
TFTIF15	HLD1506	Hosiden	1024 x 768	+5Vdc	FX8-80S-SV

TABLE Fl - TFTIF BOARDS AND THEIR DISPLAYS

The TFTIF31 and TFTIF41 boards are likely to support a number of other displays from other manufacturers, as the 31-way and 41-way connectors on the sharp display are used by a number of other manufacturers. Different displays may have different pin assignments, however, and users must carefully check the pin assignments on their displays to see that they match the pin assignments on one of the TFTIF boards.

The TFTIF, TFTIF31 and TFTIF41 boards have a solder link area to allow the selection of the correct power supply voltage for the LCD (either +5V or +3.3V). The TFTIF31, TFTIF41 and TFTIF15 boards contain power transistors which can switch off the power to the LCD when instructed to do so by the 65550 chip. This allows the display to be powered down, if required, when the TB486 is in standby or suspend modes.

The TFTIF31, TFTIF41 and TFTIF15 boards also feature a connector with the 65550 backlight enable signal (ENABKL) on it. This signal can be sent to the backlight inverter, and used to power off the backlight when instructed to do so by the 65550 chip.

The TFTIF31 and TFTIF41 include solder links which can invert the image left to right, and top to bottom. These links used together can be used to tip the picture upside down, which can be useful to improve the viewing angle on the displays.

F.2 INSTALLATION

Ensure that the TB486 has been configured with a suitable VGA BIOS - typically a BIOS which supports both CRT and TFT LCD. Different BIOSes are required for TFT displays of different resolutions. See the TB486 Utilities Disk for a discussion on programming BIOSes.

Check the solder links on the TFTIFxx board against the instructions in section F.4, F.5, F.6 or F.7.

Plug the TFTIFxx board onto the LCD.

Then plug the 40-way ribbon cable assembly onto the TFTIFxx, aligning the red pin 1 marker with the pin 1 marker on the TFTIFxx connector.

Now connect the other end of the ribbon cable to connector J10 on the TB486, again checking that pin 1 on the cable mates with pin 1 on the TB486.

Connect a backlight inverter to the TFT LCD. Take care with the backlight inverter as it produces a very high voltage (several hundred volts). You may wish to connect the enable pin on the backlight inverter to the ENABKL pin on the TFTIF31, TFTIF41 or TFTIF15 boards.

Switch on the TB486. You should see clear, crisp video on the LCD display.

F.3 CABLE LENGTHS

The TFTIFxx boards are supplied without the 40-way ribbon cable. This must be ordered separately.

Users should select a cable which is as short as practical for their application.

The TFTIF-CAB11 cable is approximately 11 inches in length. This is a compromise between reducing electrical noise on the signals (which improves as the cable length decreases) and increasing convenience (which might suggest a longer cable length).

DSP Design does not recommend longer cable lengths, but customers may find they are able to increase the cable length in practice.

Customers may order their own cables from the manufacturer, Samtec, who can make cables to any length. The Samtec part number for the 11 inch cable is:

FFSD-20-D-11-01-N

F.4 TFTIF CONNECTOR AND SOLDER LINKS

Table F2 gives the pin assignments of the TFTIF display connector.

65550 Signal	LCD Signal	Pin		LCD Signal	65550 Signal
	GND	1	2	CLOCK	SHFCLK
	GND	3	4	GND	
LP	HSYNC	5	6	VSYNC	FLM
	GND	7	8	RED 0	P18
P19	RED 1	9	10	RED 2	P20
P21	RED 3	11	12	RED 4	P22
P23	RED 5	13	14	GND	
	GND	15	16	GND	
P10	GREEN 0	17	18	GREEN 1	P11
P12	GREEN 2	19	20	GREEN 3	P13
P14	GREEN 4	21	22	GREEN 5	P15
	GND	23	24	GND	
	GND	25	26	BLUE 0	P2
P3	BLUE 1	27	28	BLUE 2	P4
P5	BLUE 3	29	30	BLUE 4	P6
P7	BLUE 5	31	32	GND	
	GND	33	34	GND	
M	ENABLE	35	36	VCC	
	VCC	37	38	N/C	
	N/C	39	40	GND	
	GND	41			

TABLE F2 - TFTIF DISPLAY PIN ASSIGNMENTS

The TFTIF has one solder link, LK1. This can be set to one of two positions. The position marked "5" is for %V LCD displays. The position marked "3.3" is for 3.3V displays. You may need to change the solder link to match your display. The LD Electronics LP121S1 uses +3.3V.

F.5 TFTIF41 CONNECTOR AND SOLDER LINKS

The TFTIF41 has three solder links.

65550 Signal	LCD Signal	Pin		LCD Signal	65550 Signal
	GND	1	2	CLOCK	SHFCLK
	GND	3	4	HSYNC	LP
FLM	VSYNC	5	6	GND	
	GND	7	8	GND	
P18	RED 0	9	10	RED 1	P19
P20	RED 2	11	12	GND	
P21	RED 3	13	14	RED 4	P22
P23	RED 5	15	16	GND	
	GND	17	18	GND	
P10	GREEN 0	19	20	GREEN 1	P11
P12	GREEN 2	21	22	GND	
P13	GREEN 3	23	24	GREEN 4	P14
P15	GREEN 5	25	26	GND	
	GND	27	28	GND	
P2	BLUE 0	29	30	BLUE 1	P3
P4	BLUE 2	31	32	GND	
P5	BLUE 3	33	34	BLUE 4	P6
P7	BLUE 5	35	36	GND	
	ENABLE	37	38	RIGHT/LEFT	
	LCD VCC	39	40	LCD VCC	
	UP/DOWN	41			

TABLE F3 - TFTIF41 DISPLAY PIN ASSIGNMENTS

LK1 can be set to one of two positions. The position marked "5" is for %V LCD displays. The position marked "3.3" is for 3.3V displays. You may need to change the solder link to match your display. The Sharp LQ12S41 uses +3.3V.

LK2 and LK3 change the display orientation. For a normal image both should be left open, or linked in the 2-3 position. For an upside-down image both should be linked in the 1-2 position.

The ENABLK signal can be taken to a backlight inverter from connector J3. J3 is a Molex 53261-0290 connector. Pin assignments are given in Table F5. ENABKL is logic 1 to turn on this inverter.

F.6 TFTIF31 CONNECTOR AND SOLDER LINKS

Table F4 gives the pin assignments of the TFTIF31 display connector.

65550 Signal	LCD Signal	Pin		LCD Signal	65550 Signal
	GND	1	2	CLOCK	SHFCLK
LP	HSYNC	3	4	VSYNC	FLM
	GND	5	6	RED 0	P18
P19	RED 1	7	8	RED 2	P20
P21	RED 3	9	10	RED 4	P22
P23	RED 5	11	12	GND	
P10	GREEN 0	13	14	GREEN 1	P11
P12	GREEN 2	15	16	GREEN 3	P13
P14	GREEN 4	17	18	GREEN 5	P15
	GND	19	20	BLUE 0	P2
P3	BLUE 1	21	22	BLUE 2	P4
P5	BLUE 3	23	24	BLUE 4	P6
P7	BLUE 5	25	26	GND	
M	ENABLE	27	28	VCC	
	VCC	29	30	LEFT/RIGHT	
	UP/DOWN	31			

TABLE F4 - TFTIF31 DISPLAY PIN ASSIGNMENTS

The TFTIF31 has three solder links.

LK1 can be set to one of two positions. The position marked “5” is for 5V LCD displays. The position marked “3.3” is for 3.3V displays. You may need to change the solder link to match your display. The Sharp LQlOD42 andLQ64D341 use +5V and the board is linked in this position by default.

LK2 and LK3 change the display orientation. For a normal image both should be left open, or linked in the 2-3 position. For an upside-down image both should be linked in the 1-2 position.

The ENABLK signal can be taken to a backlight inverter from connector J3. J3 is a Molex 53261-0290 connector. Pin assignments are given in Table F5. ENABKL is logic 1 to turn on this inverter.

J3 Pin	Signal
1	VCC
2	ENABKL
3	GND

TABLE F5 - J3 PIN ASSIGNMENTS

F.7 TFTIF15 CONNECTOR AND SOLDER LINKS

Table F6 gives the pin assignments of the TFTIF15 display connector.

The TFTIF15 has one solder link. LK1 can be set to one of two positions. In the 1-2 position the display's +5V power is sourced from the TB486 via the 40-way ribbon cable. In the 2-3 position the display's +5V supply is sourced from connector J4.

Because the Hosiden display may require significant current, DSP Design recommend that the display is powered via J4. Pin assignments of connector J4 are given in Table F6.

J3 Pin	Signal
1	+5V
2	+5V
3	GND
4	GND
5	N/C
6	VCC(from TB486)
7	ENABKL
8	GND

TABLE F6 - TFTIF1 5 Jl PIN ASSIGNMENTS

The ENABLK signal can be taken to a backlight inverter from connector J3. J3 is a Molex 53261-0290 connector. Pin assignments are given in Table F5. ENABKL is logic 1 to turn on this inverter. The ENABKL signal is also available on J4.

65550 Signal	LCD Signal	Pin		LCD Signal	65550 Signal
	GND	1	2	GND	
	GND	3	4	GND (RA0)	
	GND (RA1)	5	6	GND	
P16	RA2	7	8	RA3	P17
P18	RA4	9	10	RA5	P19
	GND	11	12	GND	
	GND	13	14	GND (GA0)	
	GND (GA1)	15	16	GND	
P8	GA2	17	18	GA3	P9
P10	GA4	19	20	GA5	P11
	GND	21	22	GND	
	GND	23	24	GND (BA0)	
	GND (BA1)	25	26	GND	
P0	BA2	27	28	BA3	P1
P2	BA4	29	30	BA5	P3
	GND	31	32	GND	
	GND	33	34	GND (RB0)	
	GND (RB1)	35	36	GND	
P20	RB2	37	38	RB3	P21
P22	RB4	39	40	RB5	P23
	GND	41	42	GND	
	GND	43	44	GND (GB0)	
	GND (GB1)	45	46	GND	
P12	GB2	47	48	GB3	P13
P14	GB4	49	50	GB5	P15
	GND	51	52	GND	
	GND	53	54	GND (BB0)	
	GND (BB1)	55	56	GND	
P4	BB2	57	58	BB3	P5
P6	BB4	59	60	BB5	P7
	GND	61	62	GND	
SHFCLK	CLK	63	64	GND	
	GND	65	66	HS	LP
	GND	67	68	GND	
ENABLE	DE	69	70	VS	FLM
	VCC	71	72	VC	
	VCC	73	74	VCC	
	VCC	75	76	N/C (TEST1)	
	GND (FRCC)	77	78	VVAC	
	VOUT	79	80	GND	

TABLE F7 - TFTIF15 PIN ASSIGNMENTS